PRODUCT SPECIFICATION

100GBASE-ZR4 QSFP28 Optical Transceiver Module

P/N: HQSFP28-DL8

Product Features

- QSFP28 MSA form factor
- Hot pluggable 38 pin electrical interface
- 4 LAN-WDM lanes MUX/DEMUX design
- 4x25G Electrical Interface
- LC duplex connector
- Supports 103.125Gb/s aggregate bit rates
- Maximum power consumption 6.5W
- Up to 80km transmission on single mode fiber
- Commercial case temperature range of 0°C to 70°C
- Single 3.3V power supply
- RoHS 2.0 compliant

Application

- 100GBASE ZR4 Ethernet
- Telecom Networking

General Description

Hi-Optel's HQSFP28-DL8 is designed for 80km optical communication applications. This module contains 4-lane optical transmitter, 4-lane optical receiver and module management block including 2 wire serial interface. The optical signals are multiplexed to a single-mode fiber through an industry standard LC connector. A block diagram is shown in Figure 1.

Transceiver Block Diagram

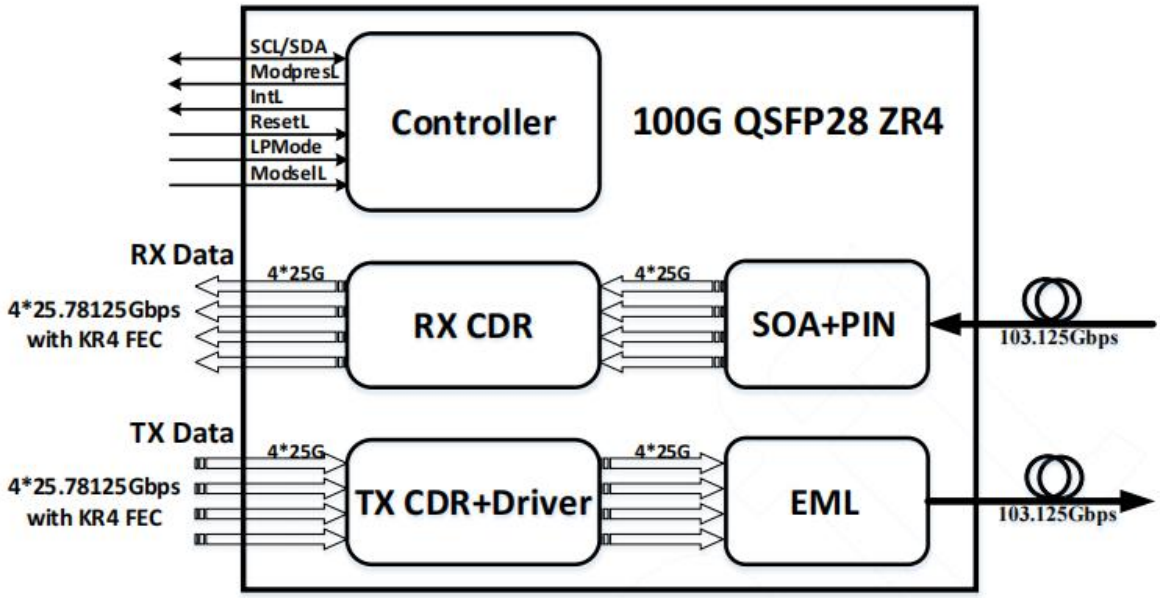

Figure 1. Transceiver Block Diagram

ModSelL:

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and deasserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL :

The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

LPMode:

The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2).

ModPrsL:

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

IntL:

IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).

Pin Definition and Description

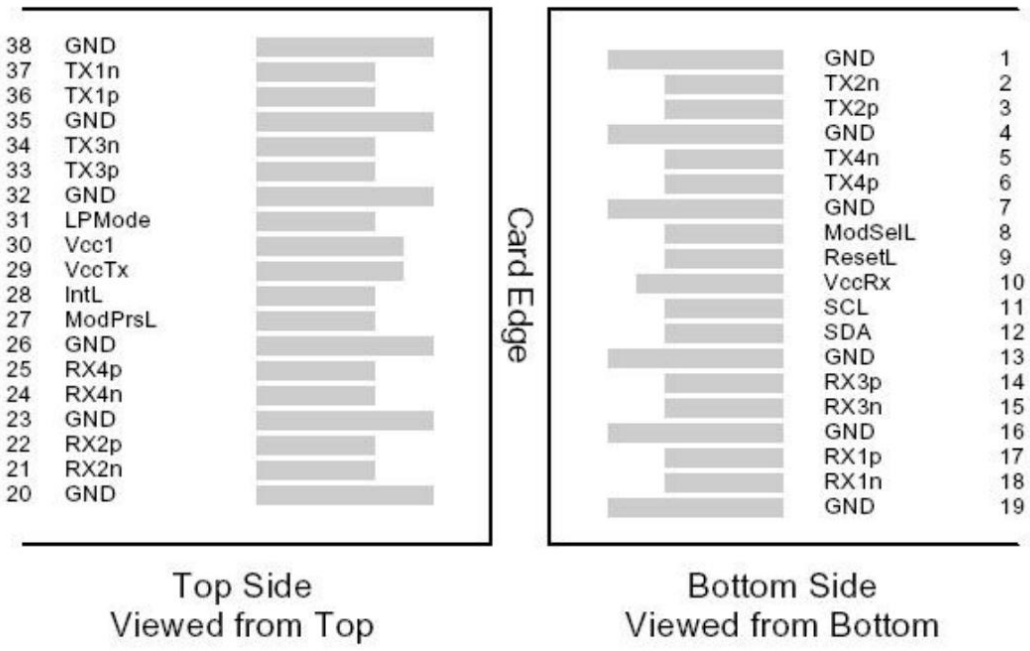

Figure 2. MSA compliant Connector(per SFF-8679)

Table 1. Pin definition and descriptions

PIN	Symbol	Description	Note
1	GND	Ground	1
2	Tx2n	CML-I Transmitter 2 Inverted Data Input	
3	Tx2p	CML-I Transmitter 2 Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	CML-I Transmitter 4 Inverted Data Input	
6	Tx4p	CML-I Transmitter 4 Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	LVTLL-I Module Select	
9	ResetL	LVTLL-I Module Reset	1
10	VCCRx	+3.3V Power Supply Receiver	
11	SCL	LVCMOS-I/O 2-Wire Serial Interface Clock	
12	SDA	LVCMOS-I/O 2-Wire Serial Interface Data	
13	GND	Ground	1
14	Rx3p	CML-O Receiver 3 Non-Inverted Data Output	
15	Rx3n	CML-O Receiver 3 Inverted Data Output	
16	GND	Ground	1
17	Rx1p	CML-O Receiver 1 Non-Inverted Data Output	
18	Rx1n	CML-O Receiver 1 Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	CML-O Receiver 2 Inverted Data Output	
22	Rx2p	CML-O Receiver 2 Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	CML-O Receiver 4 Inverted Data Output	
25	Rx4p	CML-O Receiver 4 Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VCCTx	+3.3V Power Supply Transmitter	
30	VCC1	+3.3V Power Supply	
31	LPMode	LVTLL-I Low Power Mode	
32	GND	Ground	1
33	Tx3p	CML-I Transmitter 3 Non-Inverted Data Input	
34	Tx3n	CML-I Transmitter 3 Inverted Data Input	
35	GND	Ground	1
36	Tx1p	CML-I Transmitter 1 Non-Inverted Data Input	
37	Tx1n	CML-I Transmitter 1 Inverted Data Input	
38	GND	Ground	1

Note: 1. Circuit ground is internally isolated from chassis ground.

Absolute Maximum Ratings:

Module performance is not guaranteed and reliability is not implied for any condition that beyond the operating range. Exceeding the limits below may damage the transceiver module permanently.

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	T_{ST}	-40	+85	℃	
Maximum Supply Voltage	V_{CC}	0	+3.6	V	
Relative Humidity	RH	5	85	%	1
Damage Threshold, each lane	THd	6.5		dBm	

Note: 1. No-condensing

Operating Environments:

Parameter	Symbol	Min	Typical	Max	Unit	Note
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Operating Case Temperature	T_{OP}	0		+70	℃	
Link Distance with G.652				80	km	

Electrical Characteristics:

Parameter	Symbol	Min	Typical	Max	Unit	Note
Power Consumption	P			6.5	W	
Power Supply Current	I_{CC}			1.8759	A	Steady State
Transmitter (Per Lane)						
Data Rate			25.78125		Gb/s	
Differential Voltage pk-pk	V_{pp}			900	mV	At 1MHz
Common mode Voltage	V_{CM}	-350		2850	mV	
Transition Time	T_{rise}/T_{fall}	10			ps	20%-80%
Differential Termination Resistance Mismatch				10	%	At 1MHz
Eye Width	EW15	0.46			UI	
Eye Width	EH15	95			mV	
Receiver (Per Lane)						
Data Rate			25.78125		Gb/s	
Differential Data Output Swing	$V_{out,pp}$			900	mV	
Common Mode Voltage	V_{CM}	-350		2850	mV	
Common Mode Noise,RMS	V_{RMS}			17.5	mV	
Differential Termination Resistance Mismatch				10	%	At 1MHz
Transition Time	T_{rise}/T_{fall}	12			ps	20%-80%
Eye Width	EW15	0.57			UI	
Eye Width	EH15	228			mV	

Optical Characteristics:

100GBASE-ZR4 Operation（EOL, TOP = 0 to +70 ℃ , VCC = 3.135 to 3.465 Volts）

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transmitter						
Signaling Speed per Lane		25.78125 ± 100 ppm			Gb/s	
Transmit wavelengths	L_0	1294.53	1295.56	1296.59	nm	
	L_1	1299.02	1300.05	1301.09	nm	
	L_2	1303.54	1304.58	1305.63	nm	
	L_3	1308.09	1309.14	1310.19	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	P_T	8.0		12.5	dBm	
Average Launch Power per Lane	P_{AVG}	2.0		6.5	dBm	
Difference in launch power between any two lanes(Average and OMA)				3	dBm	
Transmitter and Dispersion Penalty (TDP), each lane				2.5	dB	
Extinction Ratio	ER	6			dB	
$RIN_{20}OMA$				-130	dB/Hz	
Optical return loss tolerance				20	dB	
Transmitter reflectance				-12	dB	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				1
Average Launch Power OFF Transmitter, each Lane	P_{off}			-30	dBm	
Mask margin	%	5				1
Receiver						
Signaling Speed per Lane		25.78125 ± 100 ppm			Gb/s	
Receive wavelengths	L_0	1294.53	1295.56	1296.59	nm	
	L_1	1299.02	1300.05	1301.09	nm	
	L_2	1303.54	1304.58	1305.63	nm	
	L_3	1308.09	1309.14	1310.19	nm	
Damage Threshold per Lane	TH_d	6.5			dBm	
Average Receive Power per Lane	RXP_X	-28		-7	dBm	
Receiver power, each lane(OMA)				-7	dBm	
Receiver reflectance				-26	dB	
Receiver sensitivity (AOP), each lane				-28	dBm	2
Receiver 3 dB electrical upper cutoff				31	Ghz	

frequency, each lane						
LOS Assert	LOSA	-40			dBm	
LOS Deassert	LOSD			-29	dBm	
LOS Hysteresis	LOSH	0.5			dB	

Note: 1. Hit Ratio: $5x10^{-5}$

2. Measured with a 2^{31} -1 PRBS for BER = $5x10^{-5}$ with FEC

EEPROM Definitions

Lower Memory Map

Address	Type	Size	Name	Description	Value(Hex)	Remarks
0	R	1	Identifier	Identifier		
1	R	1	Status	Revision Compliance		
2	R	1	Status	Flat_mem/ IntL/Data_Not_Ready		
3	R	1	Interrupt Flags	Latched TX/RX LOS indicator		
4	R	1		Latched TX Adaptive EQ/TX Transmitter/Laser fault indicator		
5	R	1		Latched TX/RX CDR LOL indicator		
6	R	1		Latched temperature A/W / Initialization complete flag		
7	R	1		Latched supply voltage A/W		
8	R	1		Vendor Specific		
9-10	R	2		Latched RX power A/W		
11-12	R	2		Latched TX bias A/W		
13-14	R	2		Latched TX power A/W		
15-18	R	4		Reserved		
19-21	R	2		Vendor Specific		
22-23	R	2	Device monitors	Module temperature		
24-25	R	2		Reserved		
26-27	R	2		Supply voltage		
28-29	R	2		Reserved		
30-33	R	2		Vendor Specific		
34-35	R	2	Power monitors	RX input power, channel 1		
36-37	R	2		RX input power, channel 2		
38-39	R	2		RX input power, channel 3		
40-41	R	2		RX input power, channel 4		
42-43	R	2	LD Bias Monitors	TX bias, channel 1		
44-45	R	2		TX bias, channel 2		
46-47	R	2		TX bias, channel 3		
48-49	R	2		TX bias, channel 4		

50-51	R	2	Power monitors	TX power, channel 1		
52-53	R	2		TX power, channel 2		
54-55	R	2		TX power, channel 3		
56-57	R	2		TX power, channel 4		
58-73	R	2		Reserved		
74-81	R	2		Vendor Specific		
82-85	R	2		Reserved		
86	RW	1	Control	Tx Disable		
87	RW	1		Rx_Rate_select		
88	RW	1		Tx _Rate_select		
89~92	RW	4		Rx_Application_Select		
93	RW	1		Power		
94~97	RW	4		Tx_Application_Select		
98	RW	1		TX/RX CDR_control		
99	RW	1		Reserved		
100-104	RW	5	Free Side Device and Channel Masks	Module and Channel Masks		
105	RW	1		Vendor Specific		
106	RW	1		Vendor Specific		
107	RW	1		Reserved		
108-109	R	2	Free Side Device Properties	Most significant byte of propagation delay		
110	R	1		Advanced Low Power Mode / Far Side Managed / Min Operating Voltage		
111-112	RW	2	Assigned for use by PCI Express	PCI		
113	R	1	Free Side Device Properties	End Implementation		
114-118	RW	5		Reserved		
119-122	W	4		Password Change Entry Area		
123-126	W	4		Password Entry Area		
127	RW	1		Page Select Byte		

Upper Memory Map Page 00h

Address	Type	Size	Name	Description	Value(Hex)	Remarks
128	R	1	Identifier	Identifier Type of serial Module		

129	R	1	Ext. Identifier	Extended Identifier to free side device.Includes power classes, CLEI codes,CDR capability		
130	R	1	Connector	Code for connector type		
131	R	1	Specification compliance	10/40G/100G Ethernet Compliance Codes		
132	R	1		SONET Compliance Codes		
133	R	1		SAS/SATA Compliance Codes		
134	R	1		Gigabit Ethernet Compliant Codes		
135-136	R	2		Fibre Channel link length/Fibre Channel Transmitter Technology		
137	R	1		Fibre Channel transmission media		
138	R	1		Fibre Channel Speed		
139	R	1	Encoding	Code for serial encoding algorithm.		
140	R	1		Nominal bit rate, units of 100Mbps. For BR>25.4G, set this to FFh and use Byte 222.		
141	R	1		QSFP+ Rate Select Version 2.		
142	R	1		Link length supported for SMF fiber in km.		
143	R	1	Length	Length(OM3 50 um)		
144	R	1		Length(OM2 50 um)		
145	R	1		Length(OM1 62.5 um)		
146	R	1		Length(OM5 50 um)		
147	R	1	Device technology	Device technology		
148	R	1	Vendor name	Free side device vendor		
149	R	1				
150	R	1				
151	R	1				
152	R	1				
153	R	1				
154	R	1				
155	R	1				
156	R	1				
157	R	1				
158	R	1				
159	R	1				
160	R	1				

161	R	1				
162	R	1				
163	R	1				
164	R	1	Extended Module			
165-167	R	2	Vendor OUI			
168	R	1	Vendor PN	Part number provided by free side device vendor		
169	R	1				
170	R	1				
171	R	1				
172	R	1				
173	R	1				
174	R	1				
175	R	1				
176	R	1				
177	R	1				
178	R	1				
179	R	1				
180	R	1				
181	R	1				
182	R	1				
183	R	1				
184	R	1	Vendor Rev	Revision level for part number provided by vendor		
185	R	1				
186	R	1	Wavelength	Nominal laser wavelength (wave length=value/20 in nm)		
187	R	1				
188	R	1	Wavelength tolerance	Guaranteed range of laser wave length(+/- value) from nominal wave length. (wavelength Tol.=value/200 in nm)		
189	R	1				
190	R	1	Max case temp	Maximum case temperature in degrees C		
191	R	1	C_BASE	Check code for base ID fields		
192	R	1	Link codes	Extended Specification Compliance Codes		

193	R	1	Options	TX Input Equalization Auto Adaptive Capable not implemented, TX Input Equalization Fixed Programmable Settings implemented, RX Output Emphasis Fixed Programmable Settings implemented, RX Output Amplitude Fixed Programmable Settings implemented		
194	R	1		Tx CDR LOL Flag, Rx CDR LOL Flag, RX Squelch Disable, RX Output Disable, TX Squelch Disable, TX Squelch		
195	R	1		Memory page 02h implemented, Memory page 01h implemented, Active control of the select bits in the up per memory table is required to change rates, Tx_DISABLE and serial output implemented, Tx_FAULT signal implemented, Tx Loss of Signal implemented		
196	R	1	Vendor SN	Serial number provided by vendor		
197	R	1				
198	R	1				
199	R	1				
200	R	1				
201	R	1				
202	R	1				
203	R	1				
204	R	1				
205	R	1				
206	R	1				
207	R	1				
208	R	1				
209	R	1				
210	R	1				

211	R	1				
212	R	1	Date Code	Vendor's manufacturing date code		
213	R	1				
214	R	1				
215	R	1				
216	R	1				
217	R	1				
218	R	1				
219	R	1				
220	R	1	Diagnostic Monitoring Type	Average RX power measurement,Transmitter power measurement sup ported		
221	R	1	Enhanced Options	Indicates which optional enhanced features are implemented (if any) in the free side device.		
222	R	1	BR, nominal	Nominal bit rate per channel, units of 250Mbps.		
223	R	1	CC_EXT	Check Code for Address 192 to 222		
224	R	1	Vendor Specific			
225	R	1				
226	R	1				
227	R	1				
228	R	1				
229	R	1				
230	R	1				
231	R	1				
232	R	1				
233	R	1				
234	R	1				
235	R	1				
236	R	1				
237	R	1				
238	R	1				
239	R	1				
240	R	1	Vendor Specific			
241	R	1				
242	R	1	Vendor Specific			
243	R	1	Reserved			
244	R	1				
245	R	1				
246	R	1				

247	R	1				
248	R	1				
249	R	1				
250	R	1	Checksum			
251	R	1	Vendor Specific			
252	R	1				
253	R	1				
254	R	1				
255	R	1				

Digital Diagnostic Monitoring Functions

HQSFP28-DL8 supports the I2C-based Diagnostic Monitoring Interface (DMI) defined in document SFF-8636. The host can access real-time performance of transmitter and receiver optical power, temperature, supply voltage and bias current.

Performance Item	Related Bytes(A0[00] memory)	Monitor Error	Notes
Module temperature	22 to 23	+/-3°C	1, 2
Module voltage	26 to 27	< 3%	2
LD Bias current	42 to 49	< 10%	2
Transmitter optical power	50 to 57	< 3dB	2
Receiver optical power	34 to 41	< 3dB	2

Note: 1. Actual temperature test point is fixed on module case around Laser.

2. Full operating temperature range

Alarm and Warning Thresholds

HQSFP28-DL8 supports alarms function, indicating the values of the preceding basic performance are lower or higher than the thresholds.

Performance Item	Alarm Threshold Bytes(A0[03] memory)	Unit	Low threshold	High threshold
Temp Alarm	128 to 131	℃	-10	80
Temp Alarm	132 to 135	℃	0	70
Voltage Alarm	144 to 147	V	2.97	3.63
Voltage Alarm	148 to 151	V	3.135	3.465
TX Power Alarm	192 to 195	dBm	-4	8.2
TX Power Warning	196 to 199	dBm	-1	6.5
RX Power Alarm	176 to 179	dBm	-31	-4
RX Power Warning	180 to 183	dBm	-28	-7

Mechanical Specifications

This product is compatible with the QSFP28 Specification for pluggable form factor modules.

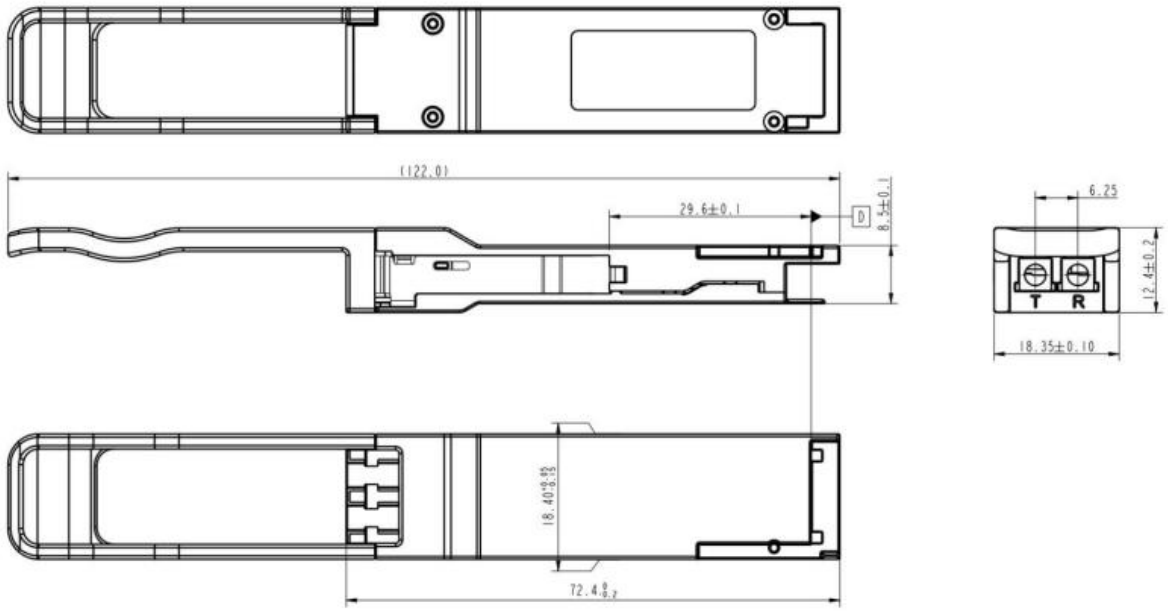

Figure 3. Mechanical Dimension (unit in mm)

Regulatory Compliance

Feature	Standard	Performance
Safety		
TUV	EN 60950-1	TUV certificate
	EN/IEC 60825-1:2007,Edition 2	
	EN/IEC 60825-1:2014,Edition 3	
	EN/IEC 60825-2:2004+A1:2006+A2:2010	
Electromagnetic Compatibility		
Radiated emissions	EMC Directive 2014/30/EU	Class B digital device with a minimum -6dB margin to the limit when tested with a metal enclosure. Final margin may vary depending on system application, good system EMI design practice, ie: suitable metal enclosure and well-bonding, is required to achieve Class B margins at the system level. Tested frequency range: 30 MHz to 40 GHz or 5th harmonic (5 times the highest frequency), whichever is less.
	EN 55032	
	CISPR 32	
	AS/NZS CISPR 32	
ESD	EN 55035	Withstands discharges of ± 8 k V contact, ±15 k V air.
	CISPR 35	
	IEC/EN 61000-4-2	

Radiated immunity	EN 55035	Field strength of 10 V/m from 80 MHz to 6 GHz.
	CISPR 35	
	IEC/EN 61000-4-3	
Restriction of Hazardous Substances		
RoHS	EU Directive 2011/65/EU (EU) 2015/863	

ESD Design

Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and otherwise handled in an ESD protected environment utilizing standard grounded benches, floor mats, and wrist straps.

Parameter	Threshold value	Notes
ESD of high-speed pins	1KV	Human Body Model
ESD of low-speed pins	2KV	Human Body Model
Air discharge during operation	15KV	
Direct contact discharges to the case	8KV	

Safety Specification Design

1) Do not look into fiber end faces without eye protection using an optical meter (such as magnifier and microscope) within 100 mm, unless you ensure that the laser output is disabled. When operating an optical meter, observe the operation requirements.

2) The RX input optical power cannot be higher than the damage threshold. You need the optical attenuator with RX in order to meet the input optical power range if necessary.

3) The HQSFP28-DL8 is the customized module, it can only interconnect with the HQSFP28-DL8 module.

CAUTION: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering Information

Part Number	Description
HQSFP28-DL8	100GBASE-ZR4 80km QSFP28, Pull-tap, refer to Figure 3

Revision History

Revision	Date	Description
Preliminary	2021/07/02	Preliminary datasheet