Features

- Supports 103.1Gb/s aggregate bit rate
- 4x25.78Gb/s retimed electrical interface
- 4x25.78Gb/s DFB-based LAN-WDM transmitter and PIN/TIA receiver
- Maximum link length of 10km on
  Single Mode Fiber (SMF)
- Hot-pluggable QSFP28 footprint
- Duplex LC receptacles
- Single3.3V power supply
- Maximum power dissipation<3.5W
- RoHS-6 compliant and lead-free
- I2C management interface
- Case operating temperature
  Commercial: 0°C to +70°C

Applications

- 100GBASE-LR4 100G Ethernet

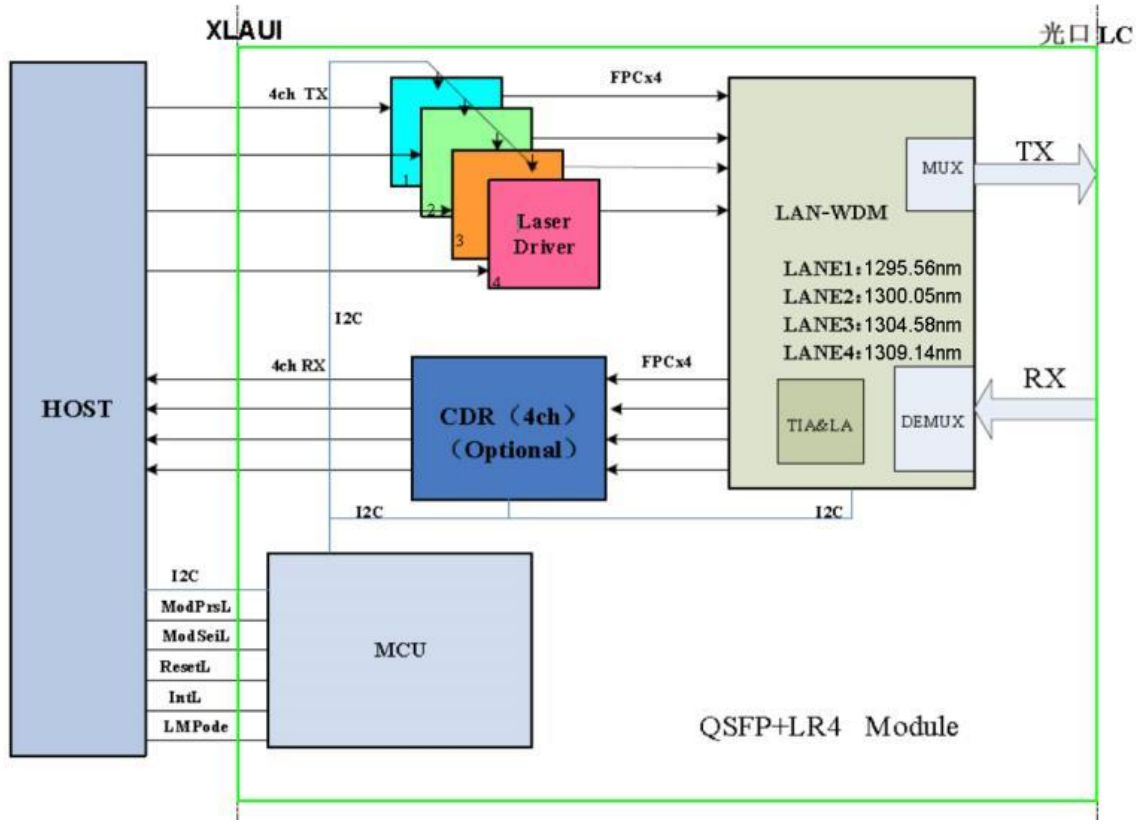
Compliance

- QSFP28 MSA.
- IEEE802.3bm and IEEE802.3ba
- SFF-8679
- RoHS

Description

The **HQSFP28-2L2** module is for use in 100 Gigabit Ethernet links over single mode fiber. They are compliant with the QSFP28 MSA and IEEE 802.3bm 100GBASE-LR4 and CAUI-4. Module-level digital diagnostic functions are available via an I2C interface, as specified by the QSFP+ MSA. The optical transceiver is compliant per the RoHS Directive 2011/65/EU.

A block diagram of QSFP28 LR4 optical transceiver is shown below



Specification

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Storage Temperature	T_S	-40		85	ºC	
Storage Ambient Humidity	H_A	5		95	%	
Maximum Supply Voltage	V_{CC}	-0.5		4.0	V	
Signal Input Voltage		-0.3		Vcc+0.3	V	
Receiver Damage Threshold		+5.5			dBm	
Lead Soldering Temperature/Time	TSOLD			260/10	ºC/sec	1
Lead Soldering Temperature/Time	TSOLD			360/10	ºC/sec	2

Note:

1. Suitable for wave soldering.
2. Only for soldering by iron.

Data Rate Specifications	Symbol	Min.	Typ.	Max.	Unit	Ref.
Bit Rate(all wavelength combined)	BR		103.1		Gb/s	1
Bit Error Ratiio@25.78Gb/s	BER			10^{-12}		2
Maximum Supported Distances				10	km	
Fiber Type			SMF			

Notes:

1. Supports 100GBASE-LR4 per IEEE 802.3ba.
2. Tested with a PRBS 2^{31}-1 test pattern.

Optical Characteristics (Condition: Ta=TOP)

Parameter	Symbol	Min	Type	Max	Unit	Note
Transmitter						
Date Rate(per channel)		25.78125 ± 100 ppm			Gb/s	
Optical Wavelength	λ_c	1294.53 1299.02 1303.54 1308.09	1295.56 1300.05 1304.58 1309.14	1296.59 1301.09 1305.63 1310.19	nm	
RMS Spectrum Width	△λ	-	-	1	nm	
Total Average Output Power	Po	-	-	10.5	dBm	
Average Output Power, each lane	P_{AVR}	-4.3		4.5	dBm	
Optical Modulation Amplitude (OMA), each lane	P_{OMA}	-1.3	-	4.5	dBm	
Optical Extinction Ratio	ER	4			dB	
Average Launch Power OFF Transmitter , each Lane	P_{OFF}			-30	dBm	
Eye Mask definition(X1,X2,X3,Y1,Y2,Y3)		{0.25,0.4,0.45,0.25,0.28,0.4}				
Receiver						
Date Rate(per channel)		25.78125 ± 100 ppm			Gb/s	
Average receive power, each lane		-10.6		4.5	dBm	
Receive power, each lane (OMA)		-8.6		4.5	dBm	
Receiver Sensitivity, each Lane(OMA)		-	-	-8.6	dBm	
Maximum Receiver Power, each lane		4.5	-	-	dBm	
LOS De-Assert	LOSD			-11.6	dBm	

LOS Assert	LOSA	-24		-13.6	dBm	
LOS Hysteresis		0.5		6	dB	
Receiver Reflectance				-26	dB	

Electrical Characteristics (Condition: Ta=TOP)

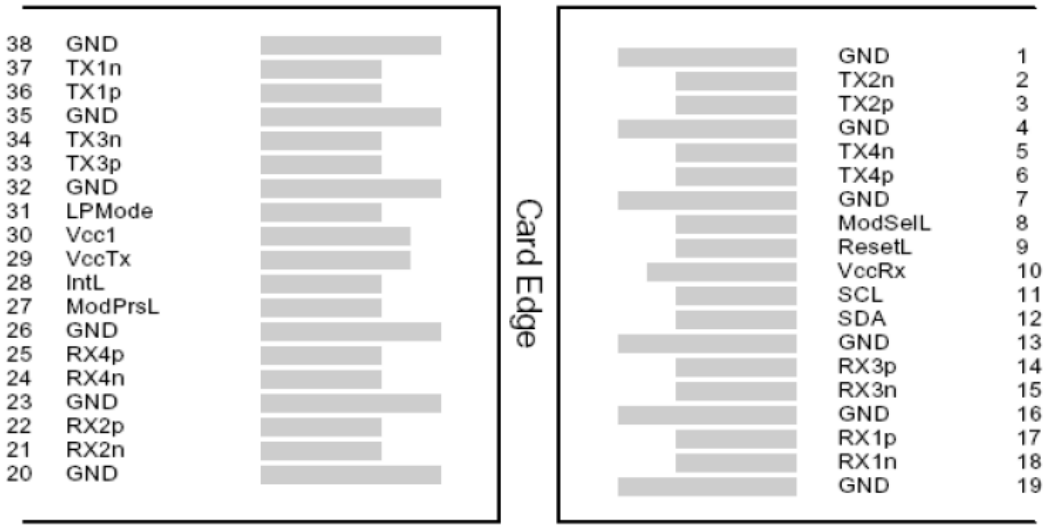
Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Supply Voltage	V_{CC}	3.135		3.465	V	
Supply Current	I_{CC}			1.12	A	
Module total power	P			3.5	W	
Transmitter						
Signaling rate per lane		25.78125±100ppm			Gb/s	
Differential pk-pk input voltage tolerance	Vin,pp,diff			900	mV	1
Differential input return loss(min)	RLd(f)	9.5 – 0.37f, 0.01≤f<8 4.75-7.4log10(f/14), 8≤f19			dB	2
Differential to common mode input return loss(min)	RLdc(f)	22-20(f/25.78), 0.01≤f<12.89 15-6(f/25.78), 12.89≤f<19			dB	2
Differential termination mismatch				10	%	
Eye width			0.46		UI	
Applied pk-pk sinusoidal Jitter		Per IEEE802.3bm Table 88-13				
Eye height			95		mV	
Receiver						
Signaling rate per lane		25.78125±100ppm			Gb/s	
Differential data output swing	Vout,pp	100		400	mVpp	3
		300		600		
		400	600	800		
		600		1200		
Eye width		0.57			UI	
Vertical eye closure	VEC			5.5	dB	
Differential output return loss (min)	RLd(f)	9.5 - 0.37f, 0.01≤f<8 4.75 - 7.4log10(f/14), 8≤f<19			dB	
Common to differential mode conversion return loss (min)	RLdc(f)	22 - 20(f/25.78), 0.01≤f<12.89 15 - 6(f/25.78), 12.89≤f<19			dB	
Differential termination mismatch				10	%	

Notes:
1) TD+/- are internally AC coupled with 100Ω differential termination inside the module.

2) fb is the data rate per lane in Gb/s
3) RD+/- outputs are internally AC coupled, and should be terminated with 100Ω (differential) at the user SERDES. Output voltage is settable in 4 discrete ranges via I2C. Default range is 400 – 800 mV.

Pin Assignment

Diagram of Host Board Connector Block Pin Numbers and Name



Pin Description

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Output	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Inverted Data Output	
15	CML-O	Rx3n	Receiver Non-Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Inverted Data Output	
18	CML-O	Rx1n	Receiver Non-Inverted Data Output	
19		GND	Ground	1

20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Output	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Output	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1

Notes:
1) GND is the symbol for single and supply (power) common for QSFP modules, all are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect theses directly to the host board signal common ground plane.
2) VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRX, Vcc1 and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for maximum current of 500mA

Digital Diagnostic Monitoring Interface

Digital diagnostics monitoring function is available on QSFP28 LR4. Real time monitoring includes Module temperature, Module supply voltage, and monitoring for each transmitter and receiver channel.
The Memory Map for QSFP28 Module is used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all QSFP28 devices. The interface has been designed largely after the XFP MSA as defined in INF-8077i Rev.4.0. The memory map has been changed in order to accommodate 4 optical channels and limit the required memory space. The single address approach is used as found in XFP. Paging is used in order to enable time critical interactions between host and Module.
The structure of the memory is shown in Figure 30. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed. For example, in table1 upper pages 01 and 02 are optional. Upper page 01 allows implementation of Application Select Table, and upper page 02 provides user read/write space. The lower page and upper page 00 are always implemented. Page 03 is required if byte 2, bit 2 in the lower page is low. See Table 39 for details regarding declaration of optional upper pages 01 and 02.

The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a “one-time-read” for all data related to an interrupt situation. After an Interrupt, IntL, has been asserted, the host can read out the flag field to determine the effected channel and type of flag.

Table 1: Digital Diagnostic Memory Map (Specific Data Field Descriptions)

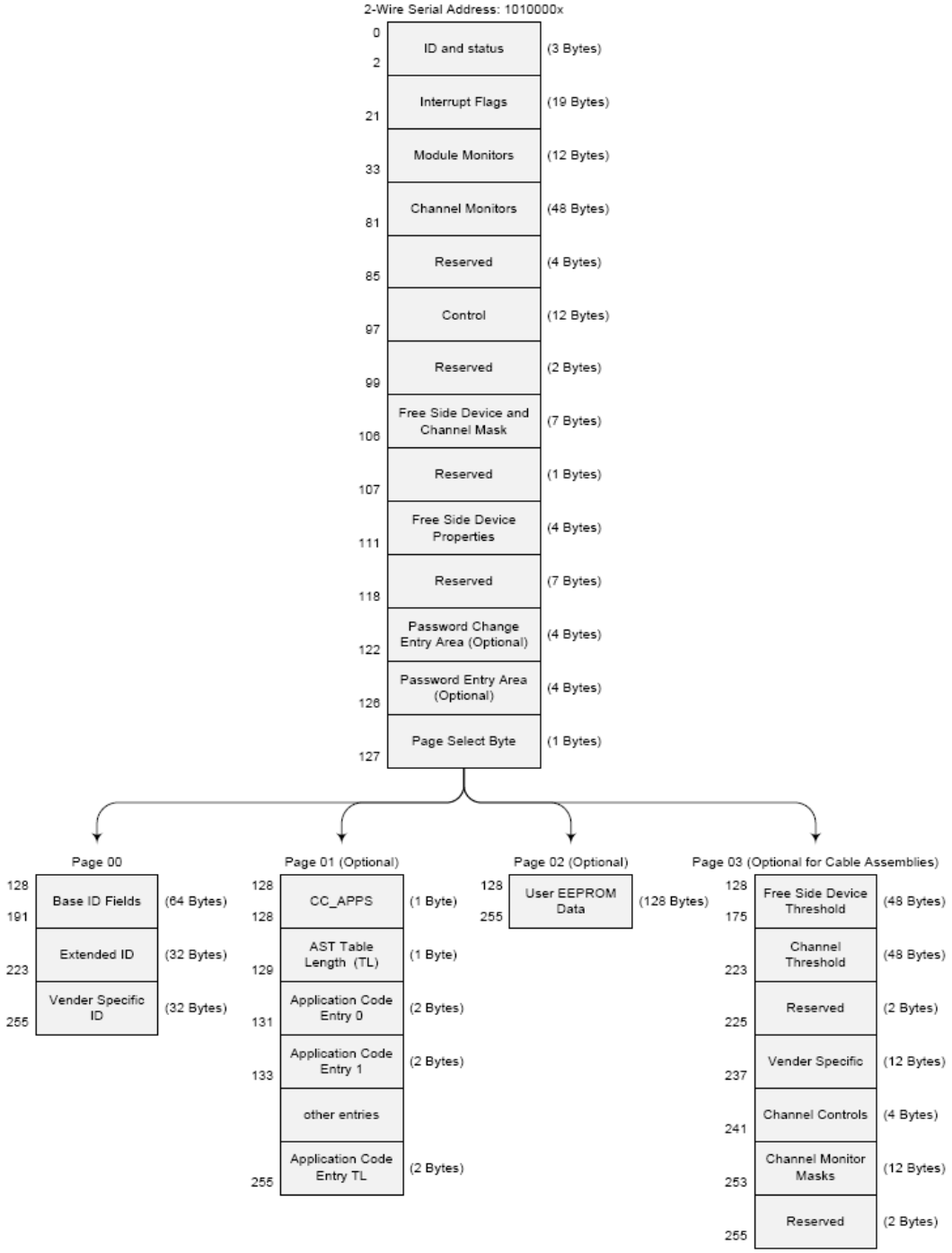


Table 2: EEPROM Serial ID Memory Contents (**A0h**)

Address	Description	Type	Passive Copper, Active Copper, Active Optical	Optical Module
0	Identifier (1 Byte)	Read-Only	R	R
1-2	Status (2 Bytes)	Read-Only	See Table 18	
3-21	Interrupt Flags (19 Bytes)	Read-Only	See Tables 19-21	
22-33	Module Monitors (12 Bytes)	Read-Only	See Table 22	
34-81	Channel Monitors (48 Bytes)	Read-Only	See Table 23	
82-85	Reserved (4 Bytes)	Read-Only	Reserved	
86-97	Control (12 Bytes)	Read/Write	See Table 24	
98-99	Reserved (2 Bytes)	Read/Write	Reserved	
100-106	Module and Channel Masks (7 Bytes)	Read/Write	See Table 25	
107-118	Reserved (12 Bytes)	Read/Write	Reserved	
119-122	Password Change Entry Area (optional) (4 Bytes)	Read/Write	O	O
123-126	Password Entry Area (optional) 4 Bytes	Read/Write	O	O
127	Page Select Byte	Read/Write	R	R

Mechanical Dimensions (Unit: mm)