Features

- ✧ Four channel full-duplex transceiver modules
- ✧ Hot pluggable QSFP form factor
- ✧ 4 x 25Gb/s DFB-based LAN-WDM Cooling transmitter
- ✧ 4 channels PIN ROSA
- ✧ Transmission data rate up to 25Gbps per channel
- ✧ Maximum link length of 2Km on G652 SMF
- ✧ Maximum Power dissipation ＜3.5W
- ✧ Duplex LC receptacles
- ✧ Single +3.3V power supply operating
- ✧ Built-in digital diagnostic functions
- ✧ Operating Case Temperature:0℃~+70℃
- ✧ RoHS-6 compliant (lead-free)

Applications

- ✧ 100GE PSM4 applications with FEC
- ✧ 25GE breakout applications

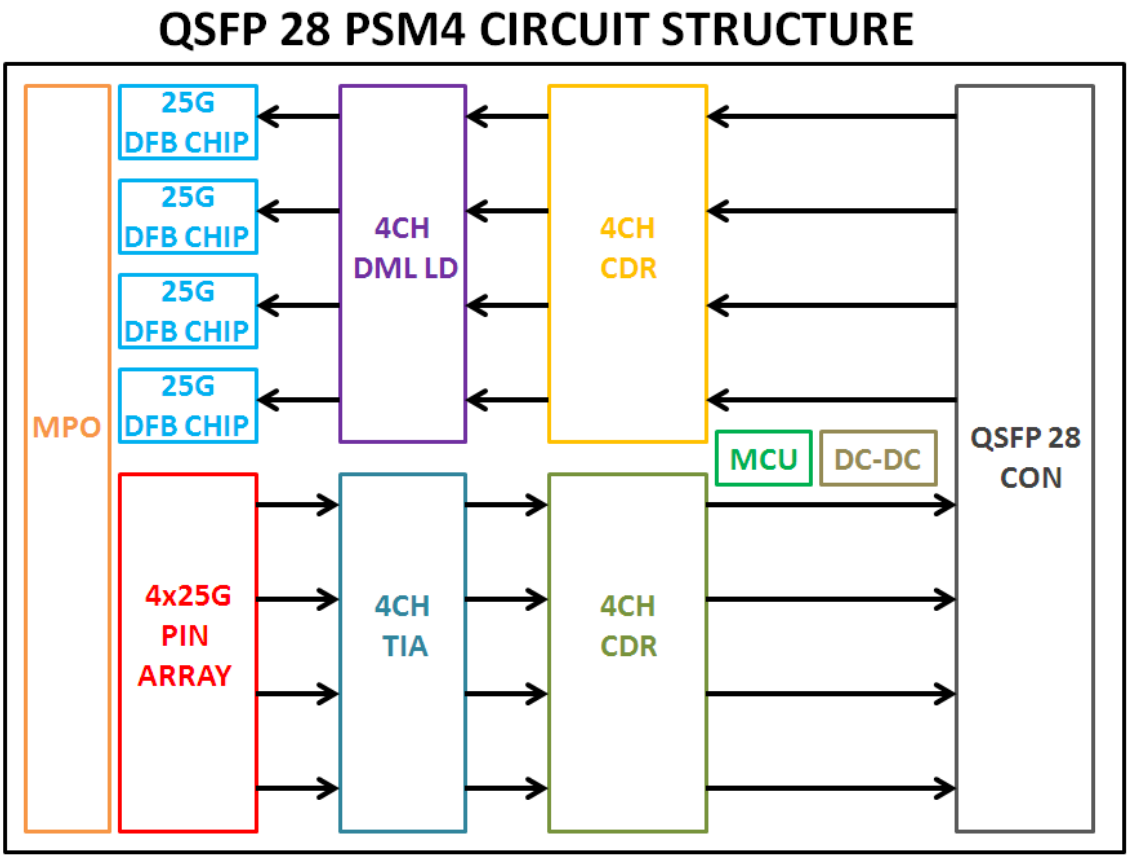
Standard

- ✧ Compliant with IEEE 802.3bm.
- ✧ Compliant with SFF-8436 QSFP+ MSA

Description

100GE PSM4 2km QSFP28 optical transceiver (HQSFP28-832) is designed for use in 100-Gigabit Ethernet links up to 2km on Single Mode Fiber (SMF). It is compliant with the QSFP28 MSA, PSM4 MSA, and portions of IEEE 802.3bm. Digital diagnostics functions are available via an I2C interface, as specified by the QSFP28 MSA. It integrates eight data lanes in each direction with 4×25.78125Gb/s bandwidth. The electrical interface uses a 38-contact edge type connector. The optical interface uses a 12-fiber MTP/MPO connector. This module incorporates Hioptel proven circuit and PSM4 technology to provide reliable long life, high performance, and consistent service.

A block diagram of QSFP+PSM4 optical transceiver is shown below



Specification

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	TST	-20	+85	℃
Operating Case Temperature	Top	0	+70	
Supply Voltage	VCC3	0.0	+3.6	V
Relative Humidity	RH	5	95	%

Recommend Operation Environment

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Supply Current	Icc			1.1	A
Operating Case temperature	Tc	0		70	℃
Data Rate Per Lane	fd		25.78125		Gb/s
Humidity	Rh	5		85	%
Power Dissipation	Pm		2	3.5	W
Link Distance with G.652	D	0.002		2	km

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Z_{in}	90	100	110	ohm
Differential Output Impedance	Z_{out}	90	100	110	ohm
Differential Input Voltage Amplitude[1]	ΔV_{in}	190		700	mVp-p
Differential Output Voltage Amplitude[2]	ΔV_{out}	300		850	mVp-p
Input Logic Level High	V_{IH}	2.0		V_{cc}	V
Input Logic Level Low	V_{IL}	0		0.8	V
Output Logic Level High	V_{OH}	V_{cc}-0.5		V_{cc}	V
Output Logic Level Low	V_{OL}	0		0.4	V

Optical Characteristics (Condition: Ta=TOP)

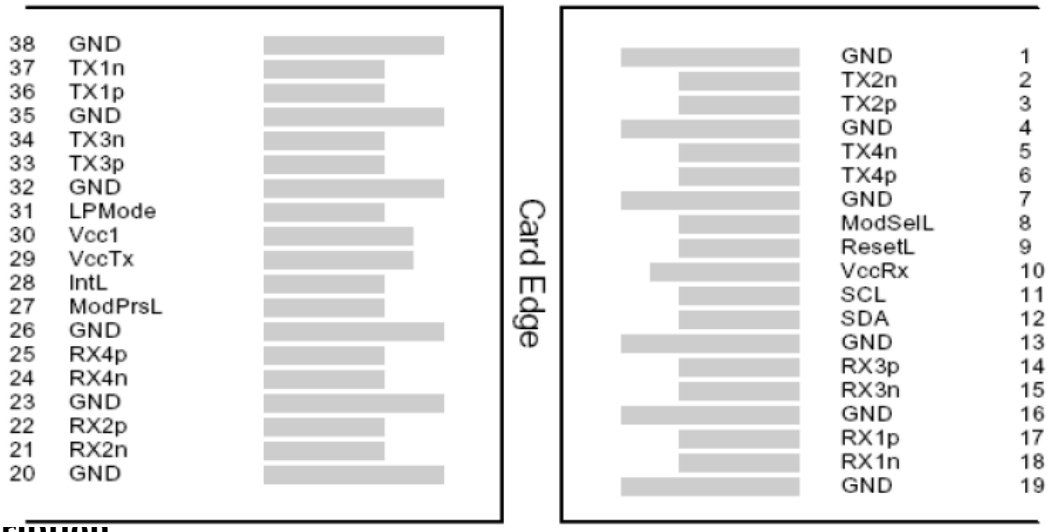
Parameter	Symbol	Min	Typical	Max	Unit
Transmitter					
Center Wavelength	λ_c	1295	1310	1325	nm
Side Mode Suppression Ratio	SMSR	30			dB
Average Launch Power (each lane)	P_{AVG}	-6		2	dBm
Optical Modulation Amplitude (each lane)	P_{OMA}	-5		2.2	dBm
Launch Power in OMA minus TDP[1] (each lane)		1.0			dBm
Transmitter and Dispersion Penalty (TDP) (each lane)	TDP			2.9	dB
Extinction Ratio	ER	3.5			dB
Relative Intensity Noise	RIN			-128	dB/Hz
Optical Return Loss Tolerance	T_{OL}			20	dB
Transmitter Reflectance	R_T			-12	dB
Average Launch Power of OFF Transmitter (each lane)	P_{OFF}			-30	dB
Eye Mask Coordinates[2]: X1, X2, X3, Y1, Y2, Y3	{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}				
Receiver					
Center Wavelength	λ_c	1295	1310	1325	nm
Damage Threshold (each lane)[3]	TH_d	3.0			dBm

Average Receive Power (each lane)		-12.66		2.0	dBm
Receiver Power (OMA) (each lane)				2.2	dBm
Receiver Reflectance	R_R			-26	dB
Receiver Sensitivity (OMA)[4] (each lane)	SEN			-11.35	dBm
LOS Assert	LOS_A		-18		dBm
LOS De-Assert – OMA	LOS_D		-15		dBm
LOS Hysteresis	LOS_H	0.5		3	dB

Even if the TDP <1dB, the OMA min must exceed the minimum value specified here.
Hit Ratio = 5×10-5.
The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
Sensitivity is specified at 5×10-5 BER at 25.78125Gb/s.

Pin Assignment

Diagram of Host Board Connector Block Pin Numbers and Name



Pin Description

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Output	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	

10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Inverted Data Output	
15	CML-O	Rx3n	Receiver Non-Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Inverted Data Output	
18	CML-O	Rx1n	Receiver Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Output	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Output	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1

Notes:
1)GND is the symbol for single and supply(power) commom for QSFP modules, All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect thess directly to the host board signal common ground plane.
2)VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRX, Vcc1 and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for maximum current of 500mA

Digital Diagnostic Monitoring Interface

Digital diagnostics monitoring function is available on QSFP28 LR4. Real time monitoring include Module temperature, Module supply voltage, and monitoring for each transmit and receive channel.

the Memory Map for QSFP28 Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all QSFP28 devices.

The structure of the memory is shown in Table 1..The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function.
The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

Table 1. Digital Diagnostic Memory Map (Specific Data Field Descriptions)

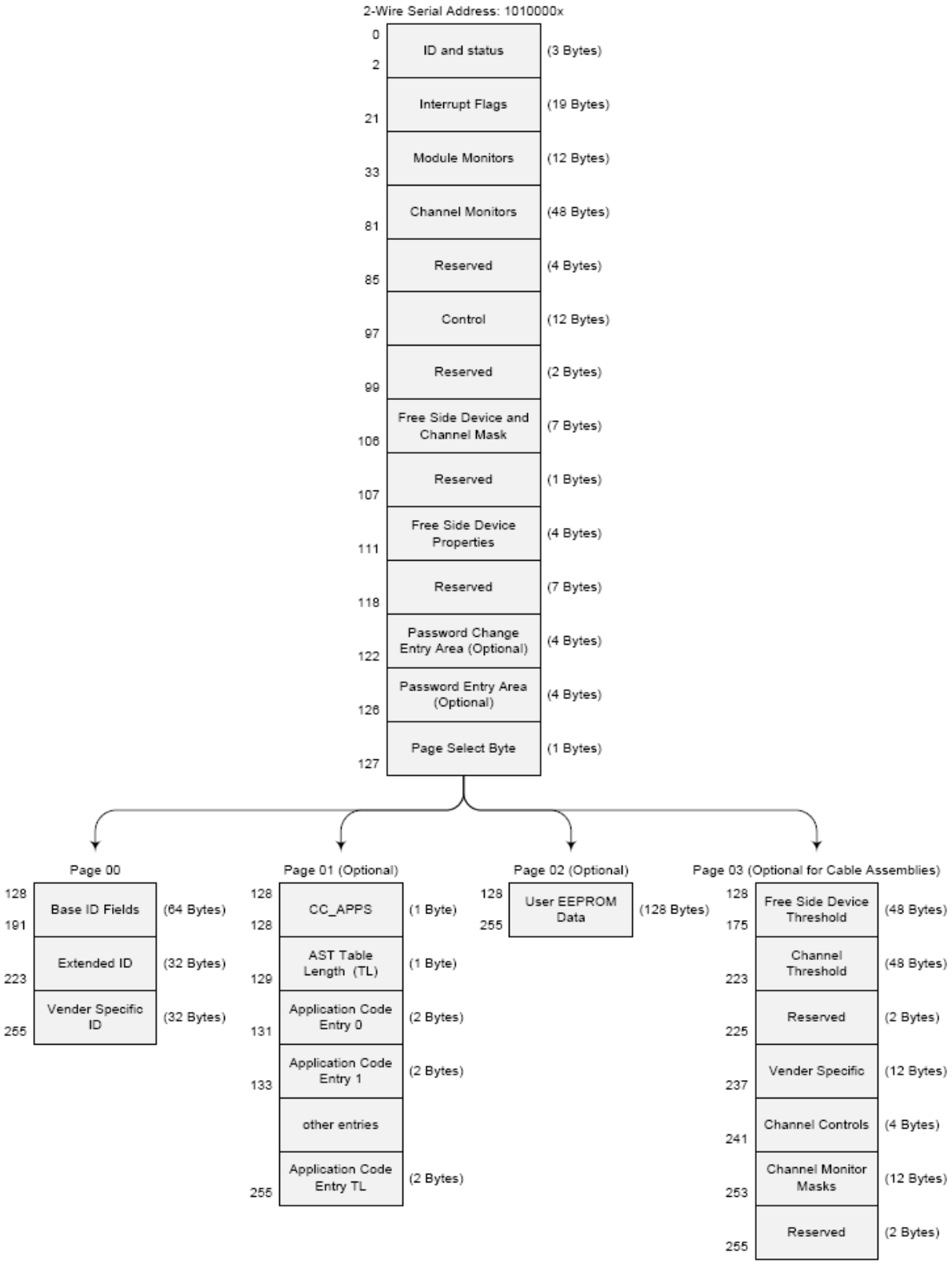
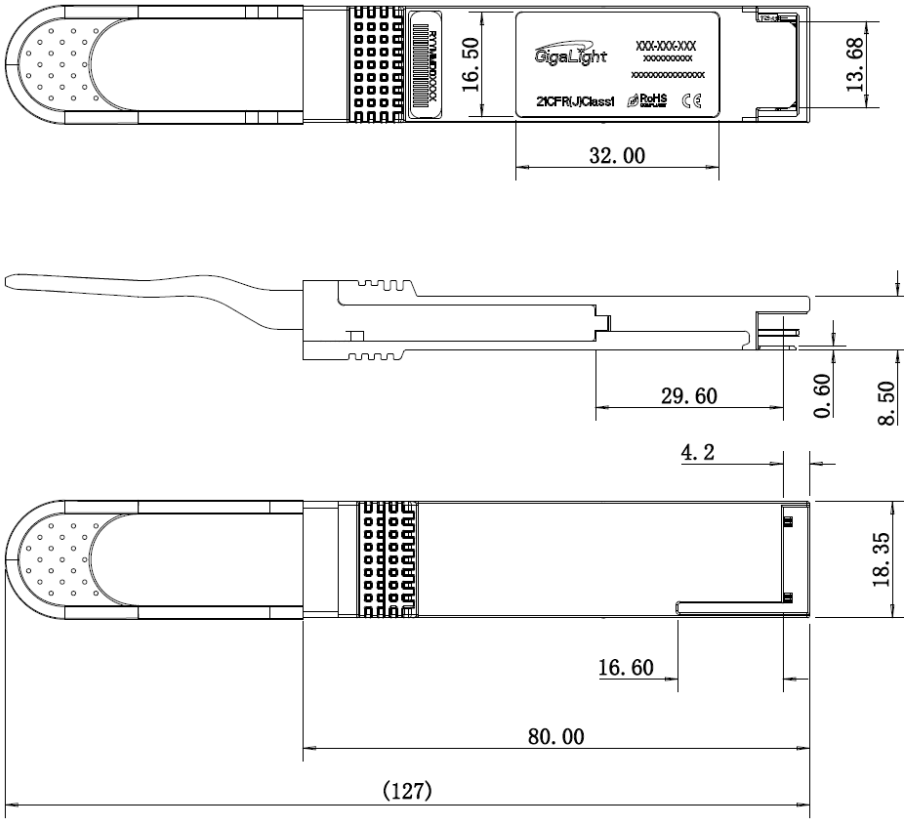


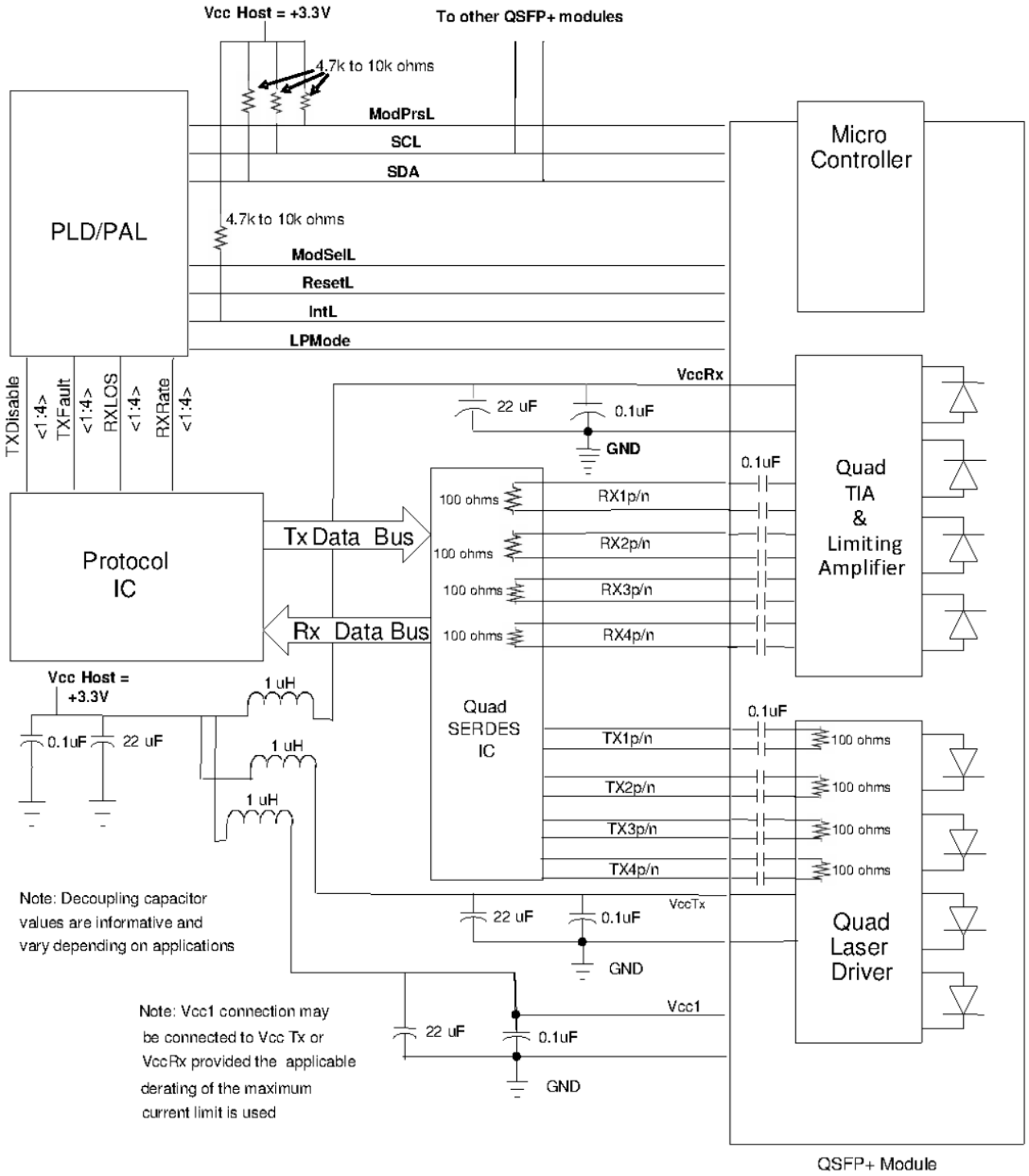
Table 2 - EEPROM Serial ID Memory Contents (**A0h**)

Address	Description	Type	Passive Copper, Active Copper, Active Optical	Optical Module
0	Identifier (1 Byte)	Read-Only	R	R
1-2	Status (2 Bytes)	Read-Only	See Table 18	
3-21	Interrupt Flags (19 Bytes)	Read-Only	See Tables 19-21	
22-33	Module Monitors (12 Bytes)	Read-Only	See Table 22	
34-81	Channel Monitors (48 Bytes)	Read-Only	See Table 23	
82-85	Reserved (4 Bytes)	Read-Only	Reserved	
86-97	Control (12 Bytes)	Read/Write	See Table 24	
98-99	Reserved (2 Bytes)	Read/Write	Reserved	
100-106	Module and Channel Masks (7 Bytes)	Read/Write	See Table 25	
107-118	Reserved (12 Bytes)	Read/Write	Reserved	
119-122	Password Change Entry Area (optional) (4 Bytes)	Read/Write	O	O
123-126	Password Entry Area (optional) 4 Bytes	Read/Write	O	O
127	Page Select Byte	Read/Write	R	R

Mechanical Dimensions



Recommended Circuit



Recommended High-speed Interface Circuit Circuit

Ordering information