Features

- ✧ Compliant to SFF-8436 QSFP+ MSA
- ✧ Compliant with 40GBASE-LR4 in IEEE802.3ba
- ✧ 4 CWDM channels operating at 10.3125 Gb/s per channel
- ✧ 64b/66b encoded data for 10GbE/40GbE applications
- ✧ Duplex LC Connector
- ✧ Up to 10 km transmission
- ✧ Maximum Power dissipation ＜2.5W
- ✧ Single +3.3V power supply operating
- ✧ Built-in digital diagnostic functions

Applications

- ✧ 40G BASE-LR4 Ethernet
- ✧ Datacom switch and router connections
- ✧ Data centers and Metro networks

Standard

- ✧ Compliant with 40G Ethernet IEEE802.3ba
- ✧ Compliant with 40GBASE-LR4 Standard
- ✧ Compliant with SFF-8436 QSFP+ MSA
- ✧ RoHS Compliant

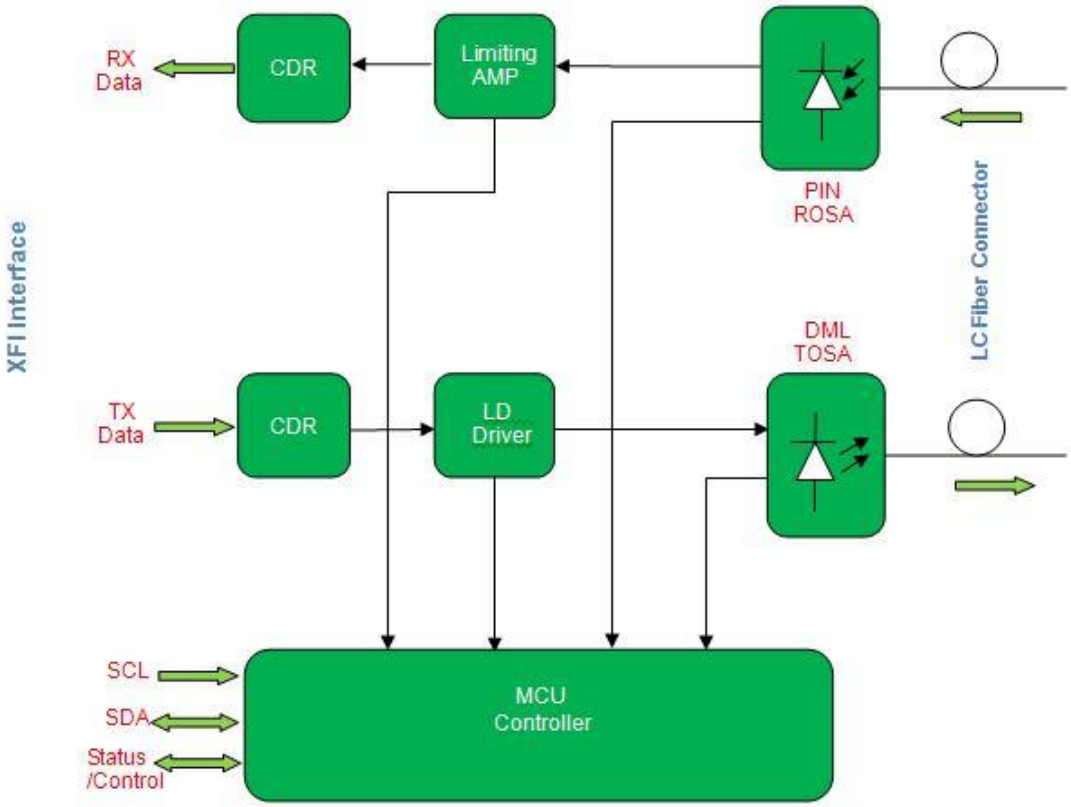
Description

The QSFP+LR4 module is a 40Gb/s optical transceiver module for serial optical communication applications, The design is compliant to 40GBASE-LR4 of the IEEE P802.3ba standard, and transmission distance up to 10 km on SMF.

The transceiver consists of two sections: Transmitter is 4 channels CWDM laser, and multiplexes them into a single channel for 40Gb/s optical transmission, CWDM laser wavelength is 1271nm,1291nm,1311nm,1331nm.Receiver is de-multiplexes a 40Gb/s optical signal into 4 CWDM channels10Gb/s signals, and converts them to 4 channels output electrical data. It contains a duplex LC

connector for the optical interface and a 38-pin connector for the electrical interface.

A block diagram of QSFP+LR4 optical transceiver is shown below



The module is hot pluggable into the 38-pin connector. The high-speed electrical interface is based on low voltage logic, with nominal 100 Ohms differential impedance and AC coupled in the module.The module have 5 low speed pins for control and status.Modseil is module select,Resetl is module reset,LPMode is Low Power Mode,Modprsl is module present,Intl is Interrupt.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{ST}	-20	+75	℃
Operating Case Temperature	T_{OP}	0	+70	℃
Supply Voltage	V_{CC3}	0.0	+3.6	V
Relative Humidity	RH	5	95	%

Recommend Operation Environment

Parameter	Symbol	Min	Typ	Max	Unit
Date Rate(per channel)			10.3125		Gb/s
Supply Voltage	V_{CC}	+3.14	3.3	+3.47	V
Supply Current(each pin)	I_{CC}			600	mA
Power Dissipation	PD			2.5	W
Operating Temperature	T_{OP}	0		+70	℃

Optical Characteristics (Condition: $T_a=T_{OP}$)

Parameter	Symbol	Min	Type	Max	Unit	Note
Transmitter						
Date Rate(per channel)			10.3125		Gb/s	
Optical Wavelength	λ0	1264.5	1271	1277.5	nm	
	λ1	1284.5	1291	1297.5	nm	
	λ2	1304.5	1311	1317.5	nm	
	λ3	1324.5	1331	1337.5	nm	
Average output power(each lane)	Po	-7		+2.3	dBm	1
Optical Modulation Amplitude, each Lane	OMA	-4	-	+3.5	dBm	
Difference in Launch Power between any two Lanes (OMA)		-	-	6.5	dB	
Optical Extinction Ratio	ER	3.5			dB	1
Optical Modulation Amplitude	OMA	-5.2			dBm	
Disabled Power	Poff	-		-30	dBm	
Side Mode Suppression Ratio	SMSR	30			dB	
Dispersion penalty each lane				2.3	dB	
Optical Return Loss Tolerance		-	-	20	dB	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Relative Intensity Noise	Rin			-128	dB/HZ	
Optical Return Loss Tolerance		-	-	12	dB	
Receiver						

Date Rate(per channel)			10.3125		Gb/s	
Receiver Sensitivity, each Lane	SR	-	-	-11.5	dBm	2
Average Power at Input, each Lane	R	-13.7		2.3	dBm	
Receiver Power (OMA), each Lane				3.5	dB	
Stressed Receiver Sensitivity in OMA each Lane				-9.9	dBm	
LOS De-Assert	LOSD			-12	dBm	
LOS Assert	LOSA	-30			dBm	
LOS Hysteresis		0.5		4	dB	
Receiver Reflectance				-26	dB	

Notes:
Note 1、 Measured at 10.3125Gb/s with PRBS 2^{31} – 1 NRZ test pattern.
Note 2、 Under the ER worst case, measured at 10.3125Gb/s with PRBS 2^{31} – 1 NRZ test pattern for BER < $1x10^{-12}$

Electrical Characteristics (Condition: $T_a=T_{OP}$)

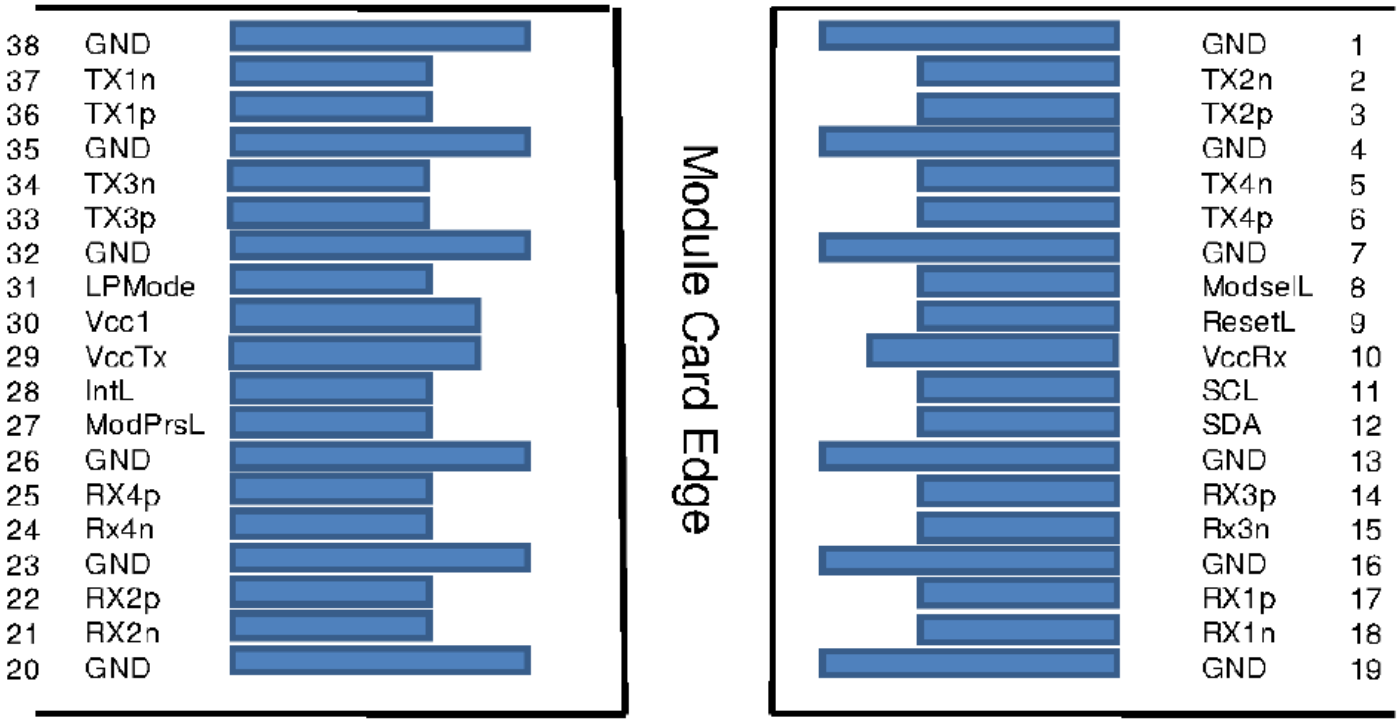
Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Current :each pin	Icc			500	mA	
Control I/O Voltage-High	VIH	2.0		Vcc	V	
Control I/O Voltage-Low	VIL	0		0.7	V	
RESETL Duration			10		Us	
RESETL De-assert time				100	ms	
Power On Time				100	ms	
Transmitter						
Differential input voltage swing	VI	150		1200	mVpp	1
C common mode voltage tolerance		15	-	-	mV	
Data Input Total Jitter,each lane	TJ			0.28	UI	
Input Differential Impedance	Zin	80	100	120	Ω	
Receiver						
Differential output voltage swing		370		900	mVpp	2
Rx Output Rise and Fall Time(20% to 80%)	Tr/Tf			35	ps	

Output Differential Impedance	Zon	80	100	120	Ω	

Note 1) TD+/- are internally AC coupled with 100Ω differential termination inside the module.
Note 2) RD+/- outputs are internally AC coupled, and should be terminated with 100Ω (differential) at the user SERDES.

Pin Assignment

Diagram of Host Board Connector Block Pin Numbers and Name



Pin Function Definitions

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Output	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1

14	CML-O	Rx3p	Receiver Inverted Data Output	
15	CML-O	Rx3n	Receiver Non-Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Inverted Data Output	
18	CML-O	Rx1n	Receiver Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Output	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Output	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1

Note

1. GND is the symbol for single and supply(power) commom for QSFP modules, All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect thess directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRX, Vcc1 and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for maximum current of 500mA

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on QSFP+ LR4. Real time monitoring include Module temperature, Module supply voltage, and monitoring for each transmit and receive channel.
the Memory Map for QSFP+ Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all QSFP+ devices. The interface has been designed largely after the XFP MSA as defined in INF-8077i Rev.4.0. The memory map has been changed in order to accommodate 4 optical channels and limit the required memory space. The single address approach is used as found in XFP. Paging is used in order to enable time critical interactions between host and Module.
The structure of the memory is shown in Figure 30. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed. For example, in table1 upper pages 01 and 02

are optional. Upper page 01 allows implementation of Application Select Table, and upper page 02 provides user read/write space. The lower page and upper page 00 are always implemented. Page 03 is required if byte 2, bit 2 in the lower page is low. See Table 39 for details regarding declaration of optional upper pages 01 and 02. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a “one-time-read” for all data related to an interrupt situation. After an Interrupt, IntL, has been asserted, the host can read out the flag field to determine the effected channel and type of flag.

Table 1. Digital Diagnostic Memory Map (Specific Data Field Descriptions)

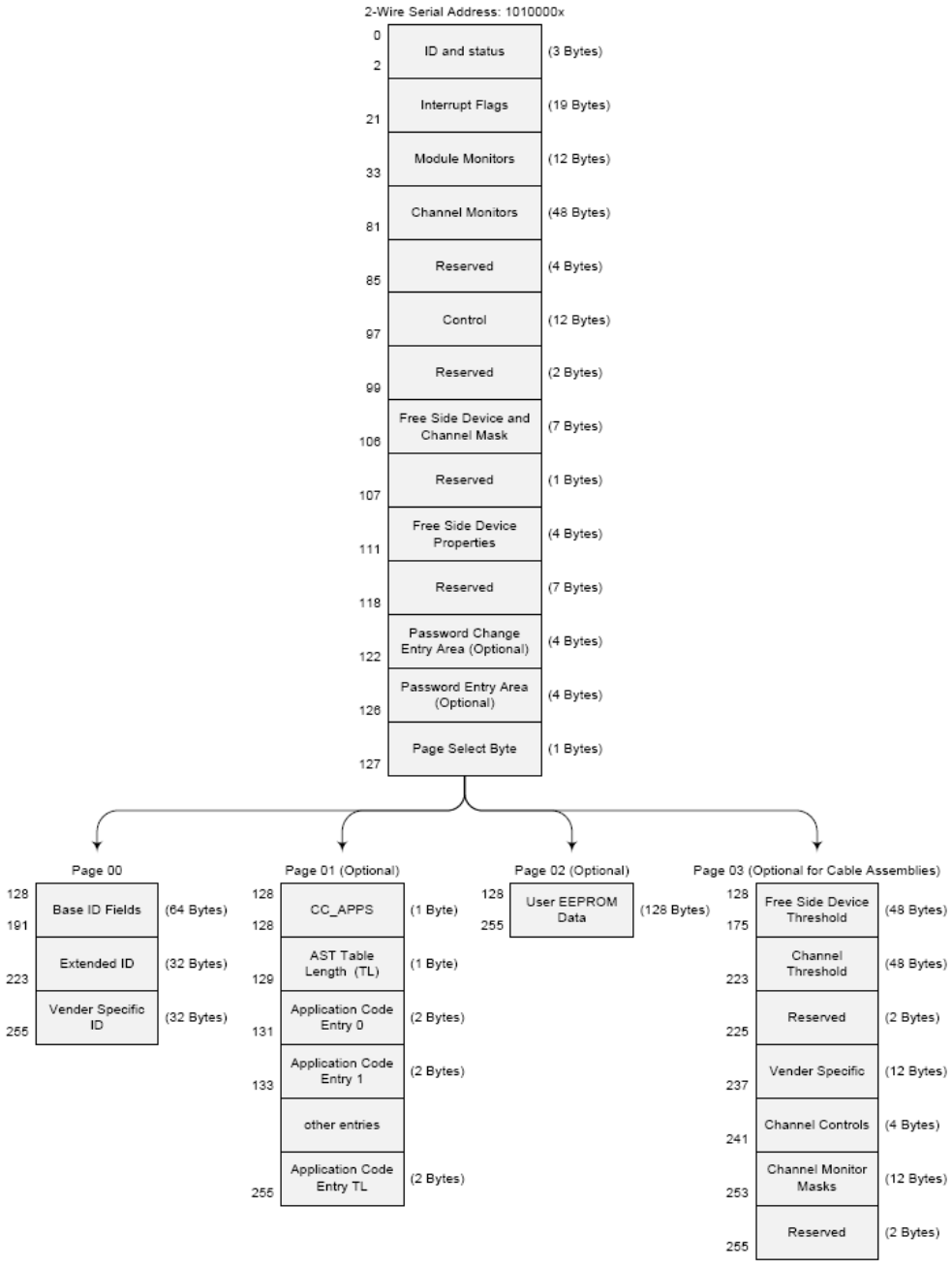


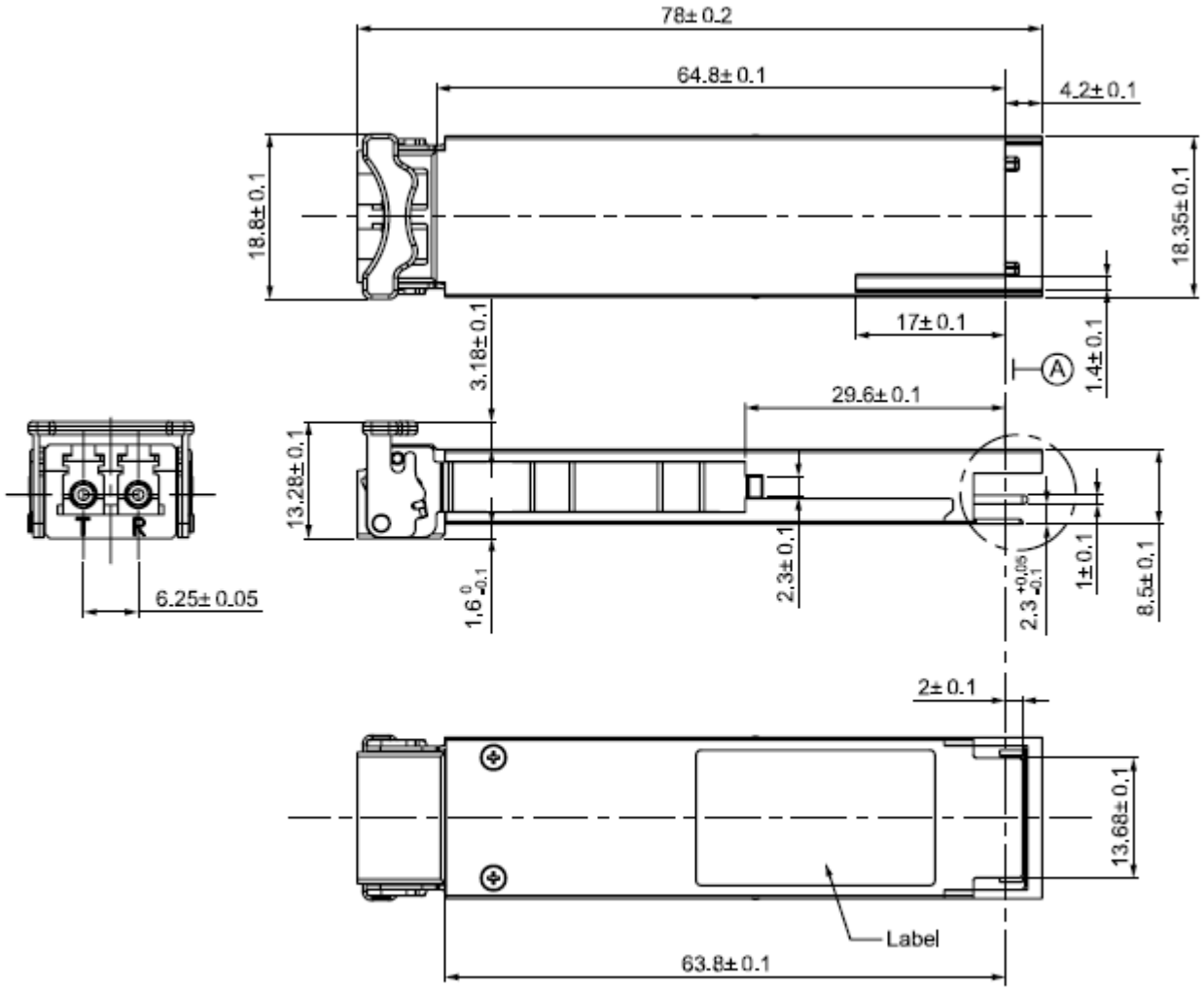
Table 2 - EEPROM Serial ID Memory Contents (**A0h**)

Address	Description	Type	Passive Copper, Active Copper, Active Optical	Optical Module
0	Identifier (1 Byte)	Read-Only	R	R
1-2	Status (2 Bytes)	Read-Only	See Table 18	
3-21	Interrupt Flags (19 Bytes)	Read-Only	See Tables 19-21	
22-33	Module Monitors (12 Bytes)	Read-Only	See Table 22	
34-81	Channel Monitors (48 Bytes)	Read-Only	See Table 23	
82-85	Reserved (4 Bytes)	Read-Only	Reserved	
86-97	Control (12 Bytes)	Read/Write	See Table 24	
98-99	Reserved (2 Bytes)	Read/Write	Reserved	
100-106	Module and Channel Masks (7 Bytes)	Read/Write	See Table 25	
107-118	Reserved (12 Bytes)	Read/Write	Reserved	
119-122	Password Change Entry Area (optional) (4 Bytes)	Read/Write	O	O
123-126	Password Entry Area (optional) 4 Bytes	Read/Write	O	O
127	Page Select Byte	Read/Write	R	R

Digital Diagnostic Monitor Characteristics

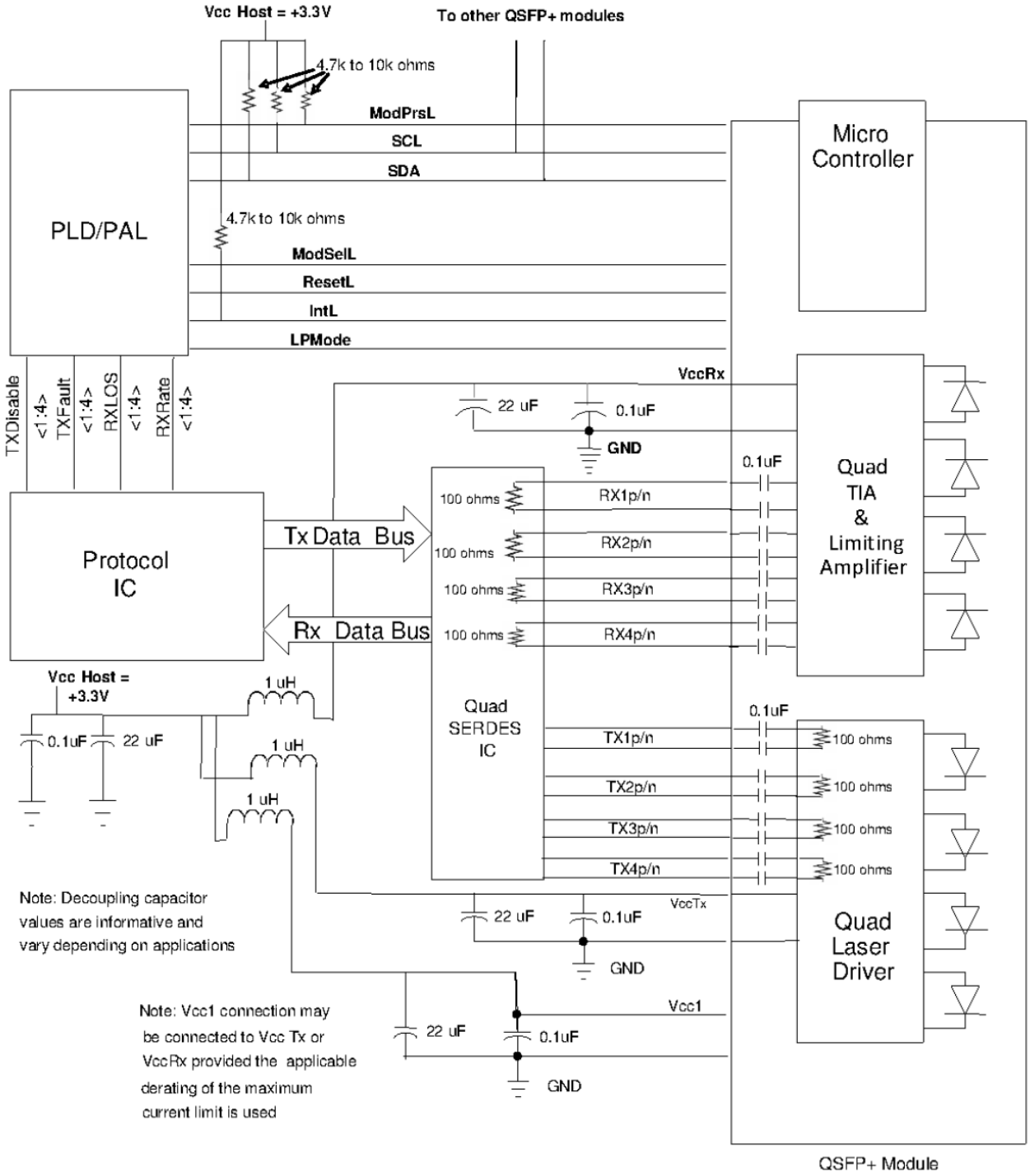
Parameter	Symbol	Min.	Max	Unit
Temperature monitor absolute error	DMI_Temp	-3	3	°C
RX power monitor absolute error	DMI_RX	-3	3	dBm
Supply voltage monitor absolute error	DMI_VCC	-0.1	0.1	V
Bias current monitor	DMI_Ibias	-10%	10%	mA

Mechanical Dimensions



QSFP LR4 Transceiver
(Unit: mm View:)

Recommended Circuit



Recommended High-speed Interface Circuit Circuit