Features

- ✧ Full duplex 4 channel 1310nm parallel module(PSM LR4)
- ✧ Data rate up to 11.1Gbps per channel
- ✧ Maximum link length of 10Km on G.652
- ✧ Hot pluggable QSFP+ form factor
- ✧ Four channel 1310nm DFB laser
- ✧ Four channel PIN detector Array
- ✧ Maximum Power dissipation:＜3.5W
- ✧ Single male MPO(APC 8-degree)connector receptacle
- ✧ Single +3.3V power supply operating
- ✧ Built-in digital diagnostic functions
- ✧ Operating Case Temperature：0℃~+70℃
- ✧ RoHS-6 compliant (lead-free)

Applications

- ✧ Infiniband Connectivity SDR/DDR/QDR
- ✧ 10GBASE-LR/W 10G Ethernet
- ✧ 2/4/8 Gbps Fiber Channel
- ✧ Data Centers and Storage Arrays
- ✧ Other Optical Links

Standard

- ✧ Compliant with 40G Ethernet IEEE802.3ba
- ✧ Compliant with SFF-8436 QSFP+ MSA

Description

QSFP PSM LR4 are a high performance, low power consumption, long reach interconnect solution supporting 40G Ethernet, fiber channel and PCIe. It is compliant with the QSFP MSA and IEEE 802.3ae 10GBASE-LR/LW3. QSFP PSM LR4 is an assembly of 4 full-duplex lanes, where each lane is capable of transmitting data at rates up to 11.1Gb/s, providing an aggregated rate of 40Gb/s.

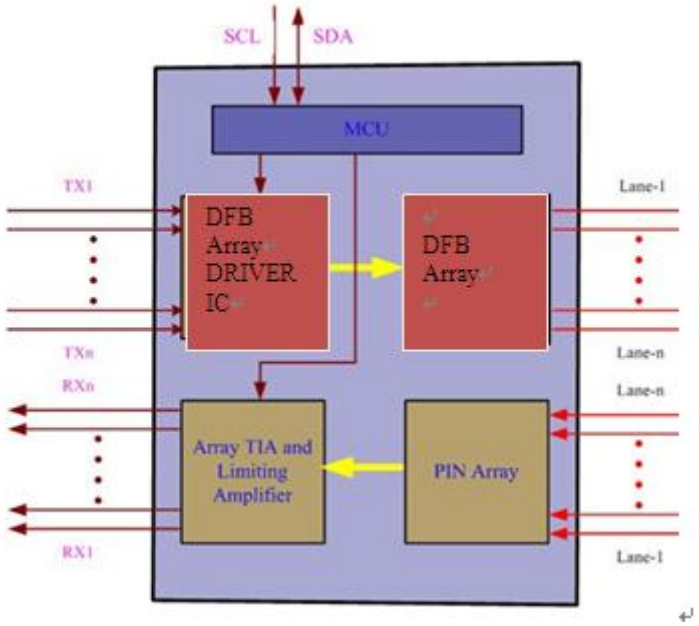


Figure1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	TST	-20	+85	℃
Operating Case Temperature	Top	0	+70	℃
Supply Voltage	VCC3	-0.3	+3.6	V
Relative Humidity(non-condensing)	RH	5	95	%

Recommend Operation Environment

Parameter	Symbol	Min	Typ	Max	Unit
Date Rate(per channel)		9.95	-	11.1	Gb/s
Supply Voltage	VCC	3.13	3.3	3.47	V
Humidity	RH	5	-	85	%
Power Dissipation	PD	-	-	3.5	W
Operating Case Temperature	TOP	0	-	+70	℃
Link Distance with G652	L	0.5	-	10000	m

Specification

Optical Characteristics (Condition: Ta=TOP)

Parameter	Symbol	Min	Type	Max	Unit	Note
Transmitter						
Optical Wavelength	λc	1290	1310	1320	nm	
SMSR		30	-	-	dB	
Transmit OMA per Lane	TxOMA	-5.2	-	3.0	dBm	
Average output power, each lane	Po	-8.2	-	0.5	dBm	1
Difference in Launch Power between any two Lanes (OMA)	Ptx,diff	-	-	6.5	dB	
Optical Extinction Ratio	ER	3.5			dB	1
Dispersion penalty, each lane				2.6	dB	
Optical Return Loss Tolerance		-	-	12	dB	
Average Launch Power OFF Transmitter , each Lane	Poff			-30	dBm	
Eye Mask definition(X1,X2,X3,Y1,Y2,Y3)		SPECIFICATION VALUES 0.25, 0.4, 0.45, 0.25, 0.28, 0.4			Hit Ratio = 5x10-5	
Receiver						
Optical Wavelength	λc	1290	1310	1330	nm	
Stressed receiver sensitivity in OMA, each lane		-	-	-10.3	dBm	1
Maximum Receiver Power, each lane		0.5	-	-	dBm	
Receiver sensitivity in OMA, each lane(PRBS 2^31-1 and BER=10^-12)				-12.6	dBm	2
Difference in Receive Power between any Two Lanes(OMA)				7.5	dBm	
LOS De-Assert	LOSD			-17	dBm	
LOS Assert	LOSA	-30			dBm	
LOS Hysteresis		0.5			dB	
Receiver Reflectance				-26	dB	

Notes:
Note 1) Measured with conformance test signal at TP3 for BER = 1E-12
Note 2) 10GBASE-LR spec .

Electrical Characteristics (Condition: Ta=TOP)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Bit Error Rate	BER	-	-	1E-12		1
Control I/O Voltage-High	VIH	2.0		Vcc	V	
Control I/O Voltage-Low	VIL	0		0.8	V	
Skew	SW	-	-	300	ps	
Transmitter						
Differential input voltage swing	VI	350		1200	mVpp	2
Input Differential Impedance	Zin	90	100	110	Ω	
Receiver						
Differential output voltage swing		425		1600	mVpp	3
Output Differential Impedance	Zon	90	100	110	Ω	

Notes:
1) BER=10^-12; PRBS 2^31-1.
2) Differential input voltage amplitude is compliant with theIEEE802.3 Annex 86A and SFF8436,and it is measured at TP1 .
3) Differential output voltage amplitude is compliant with theIEEE802.3 Annex 86A and SFF8436,and it is measured at TP4 .

Pin Assignment

Diagram of Host Board Connector Block Pin Numbers and Name

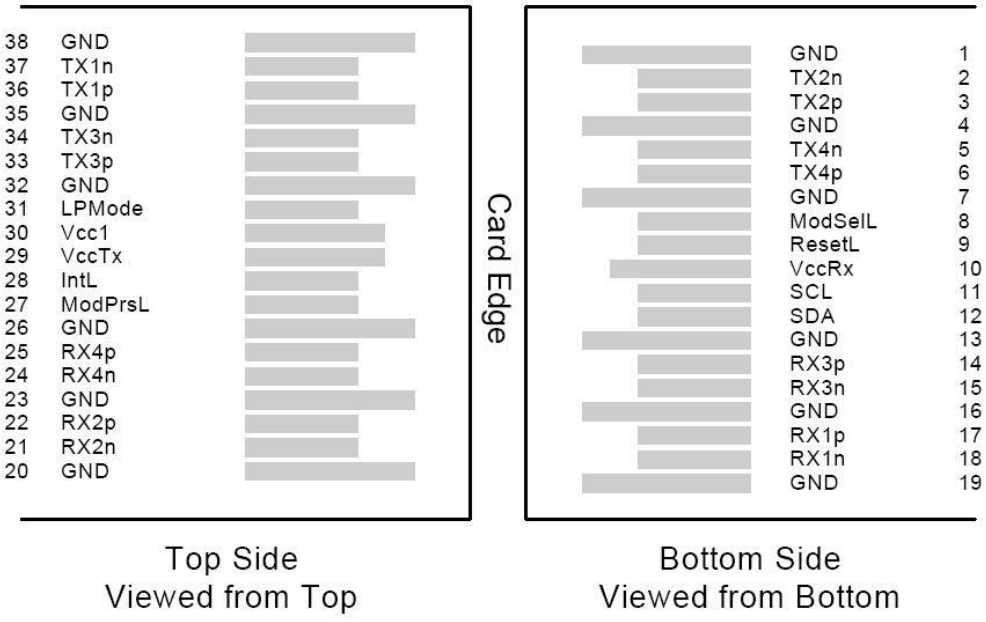


Figure2. Electrical Pin-out Details

Pin Description

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Output	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Inverted Data Output	
15	CML-O	Rx3n	Receiver Non-Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Inverted Data Output	
18	CML-O	Rx1n	Receiver Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	3
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Output	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Output	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1

Notes:
1)GND is the symbol for single and supply(power) commom for QSFP modules, All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect this pin directly to the host board signal common ground plane.
2)VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRX, Vcc1 and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for maximum current of 500mA
3)Hioptel QSFP PSM LR4 operate in the low power mode (less than 1.5 W power consumption)
This pin active high will decrease power consumption to less than 1W.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.

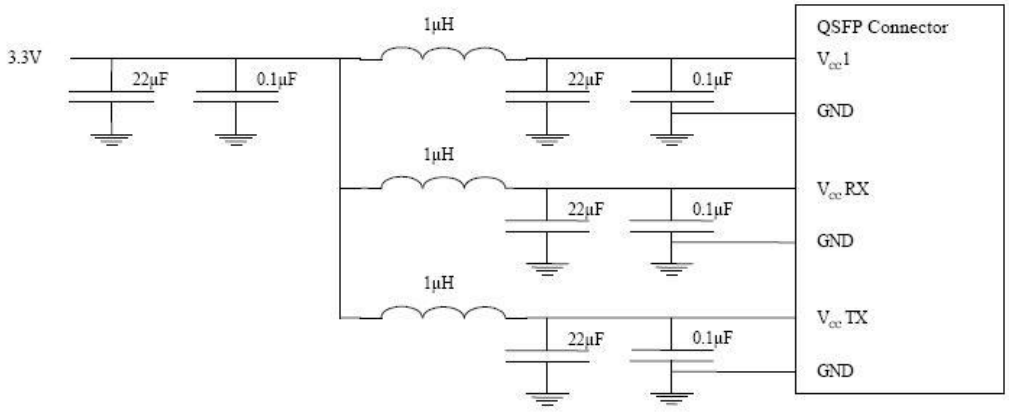
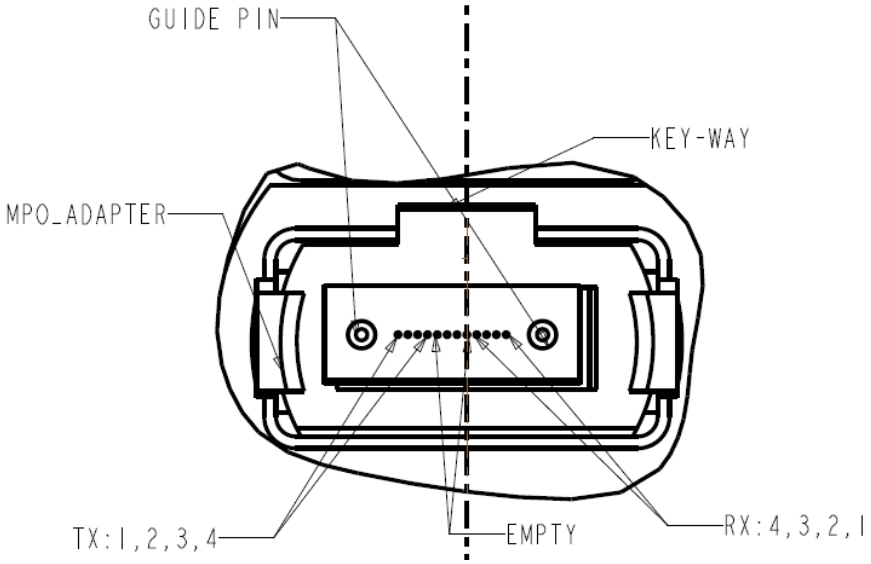


Figure3. Host Board Power Supply Filtering

40G QSFP+ PSM LR4 10km Optical Interface



Digital Diagnostic Monitoring Interface (optional)

Digital diagnostics monitoring function is available on all Hioptel QSFP+ modules. A 2-wire serial interface provides user to contact with module.

The structure of the memory is shown in Figure 4. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function.

The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

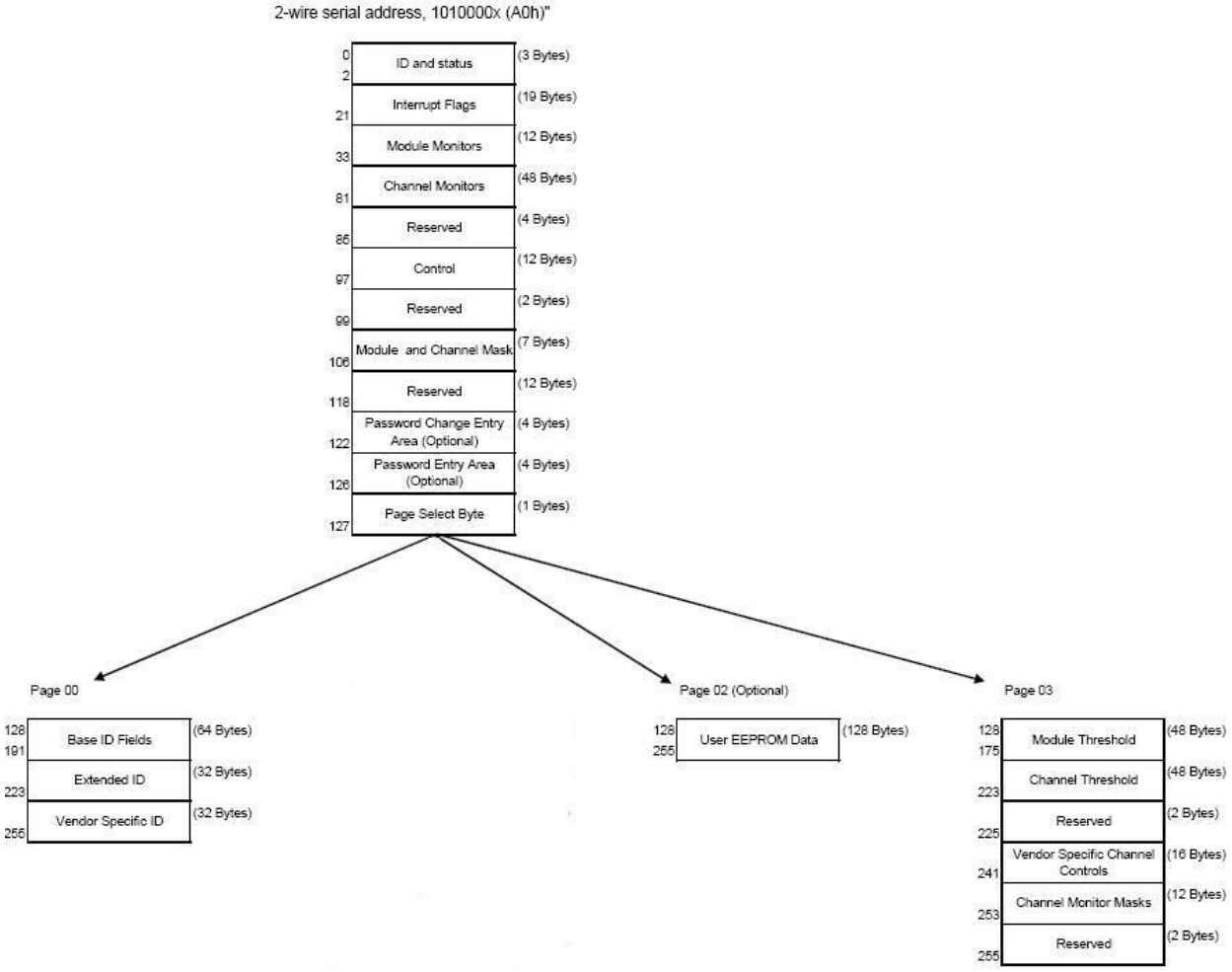


Figure4. QSFP Memory Map

Byte Address	Description	Type
0	Identifier (1 Byte)	Read Only
1-2	Status (2 Bytes)	Read Only
3-21	Interrupt Flags (31 Bytes)	Read Only
22-33	Module Monitors (12 Bytes)	Read Only
34-81	Channel Monitors (48 Bytes)	Read Only
82-85	Reserved (4 Bytes)	Read Only
86-97	Control (12 Bytes)	Read/Write
98-99	Reserved (2 Bytes)	Read/Write
100-106	Module and Channel Masks (7 Bytes)	Read/Write
107-118	Reserved (12 Bytes)	Read/Write
119-122	Reserved (4 Bytes)	Read/Write
123-126	Reserved (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

Figure5. Low Memory Map

Byte Address	Description	Type
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225	Reserved (2 Bytes)	Read Only
226-239	Reserved (14 Bytes)	Read/Write
240-241	Channel Controls (2 Bytes)	Read/Write
242-253	Reserved (12 Bytes)	Read/Write
254-255	Reserved (2 Bytes)	Read/Write

Figure6. Page 03 Memory Map

Address	Name	Description
128	Identifier (1 Byte)	Identifier Type of serial transceiver
129	Ext. Identifier (1 Byte)	Extended identifier of serial transceiver
130	Connector (1 Byte)	Code for connector type
131-138	Transceiver (8 Bytes)	Code for electronic compatibility or optical compatibility
139	Encoding (1 Byte)	Code for serial encoding algorithm
140	BR, nominal (1 Byte)	Nominal bit rate, units of 100 Mbits/s
141	Extended RateSelect Compliance (1 Byte)	Tags for Extended RateSelect compliance
142	Length SMF (1 Byte)	Link length supported for SM fiber in km
143	Length E-50 μm (1 Byte)	Link length supported for EBW 50/125 μm fiber, units of 2 m
144	Length 50 μm (1 Byte)	Link length supported for 50/125 μm fiber, units of 1 m
145	Length 62.5 μm (1 Byte)	Link length supported for 62.5/125μm fiber, units of 1 m
146	Length copper (1 Byte)	Link length supported for copper, units of 1 m
147	Device Tech (1 Byte)	Device technology
148-163	Vendor name (16 Bytes)	QSFP vendor name (ASCII)
164	Extended Transceiver (1 Byte)	Extended Transceiver Codes for InfiniBand†
165-167	Vendor OUI (3 Bytes)	QSFP vendor IEEE vendor company ID
168-183	Vendor PN (16 Bytes)	Part number provided by QSFP vendor (ASCII)
184-185	Vendor rev (2 Bytes)	Revision level for part number provided by vendor (ASCII)
186-187	Wavelength (2 Bytes)	Nominal laser wavelength (Wavelength = value / 20 in nm)
188-189	Wavelength Tolerance (2 Bytes)	Guaranteed range of laser wavelength (+/- value) from Nominal wavelength (Wavelength Tol. = value / 200 in nm)
190	Max Case Temp (1 Byte)	Maximum Case Temperature in Degrees C
191	CC_BASE (1 Byte)	Check code for Base ID fields (addresses 128-190)
192-195	Options (4 Bytes)	Rate Select, TX Disable, TX Fault, LOS
196-211	Vendor SN (16 Bytes)	Serial number provided by vendor (ASCII)
212-219	Date code (8 Bytes)	Vendor's manufacturing date code
220	Diagnostic Monitoring Type (1 Byte)	Indicates which type of diagnostic monitoring is implemented
221	Enhanced Options (1 Byte)	Indicates which optional enhanced features are implemented
222	Reserved (1 Byte)	Reserved
223	CC_EXT	Check code for the Extended ID Fields (addresses 192-222)
224-255	Vendor Specific (32 Bytes)	Vendor Specific EEPROM

Figure7. Page 00 Memory Map

Page02 is User EEPROM and its format decided by user.
The detail description of low memory and page00.page03 upper memory please see SFF-8436 document.

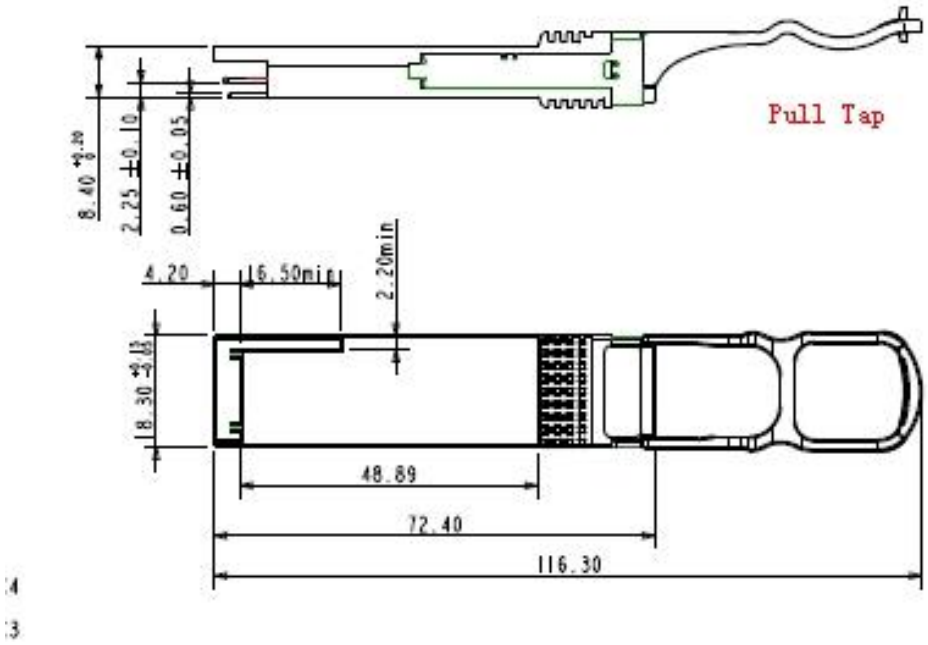
Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on[2], hot plug or rising edge of Reset until the module is fully functional[3]This time does not apply to non-Power Level 0 modules in the Low Power State
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on[2] until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on[2] to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional[3]
LPMode Assert Time	ton_LPMode	100	μs	Time from assertion of LPMode (Vin:LPMode = Vih) until module power consumption enters lower Power Level 1
LPMode Deassert Time	Toff_LPMode	300	ms	Time for deassertion of LPMode (Vin:LPMode=Vil) until module is fully functional3,5
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	μs	Time from clear on read[4] operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set (value=1b) and IntL asserted
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set(value=1b)[1] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared (value=0b)[1] until associated IntlL operation resumes
Application or Rate Select Change Time	t_ratesel	100	μs	Time from change of state of Application or Rate Select Bit[1] until transmitter or receiver bandwidth is in conformance with appropriate specification
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set (value=1b)[1] until module power consumption enters lower Power Level 1
Power_over-ride or Power-set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared(value=0b)[1] until the module is fully functional[3]

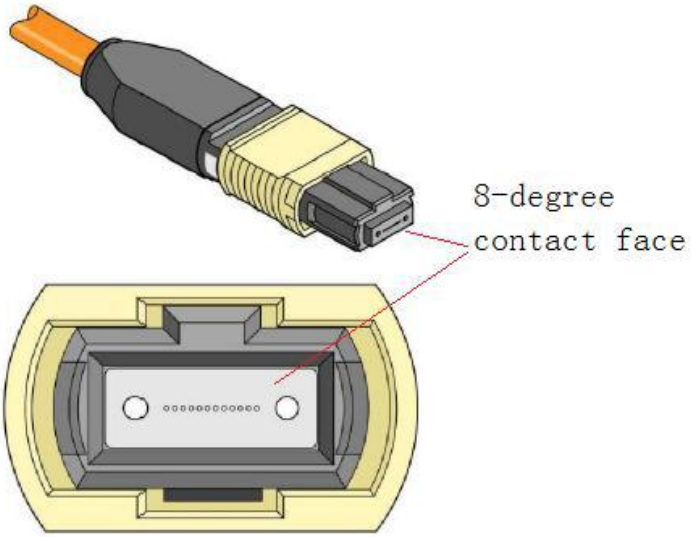
Note：

1). Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2). Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.
3). Measured from falling clock edge after stop bit of read transaction.
4). Measured from falling clock edge after stop bit of write transaction.

Mechanical Dimensions

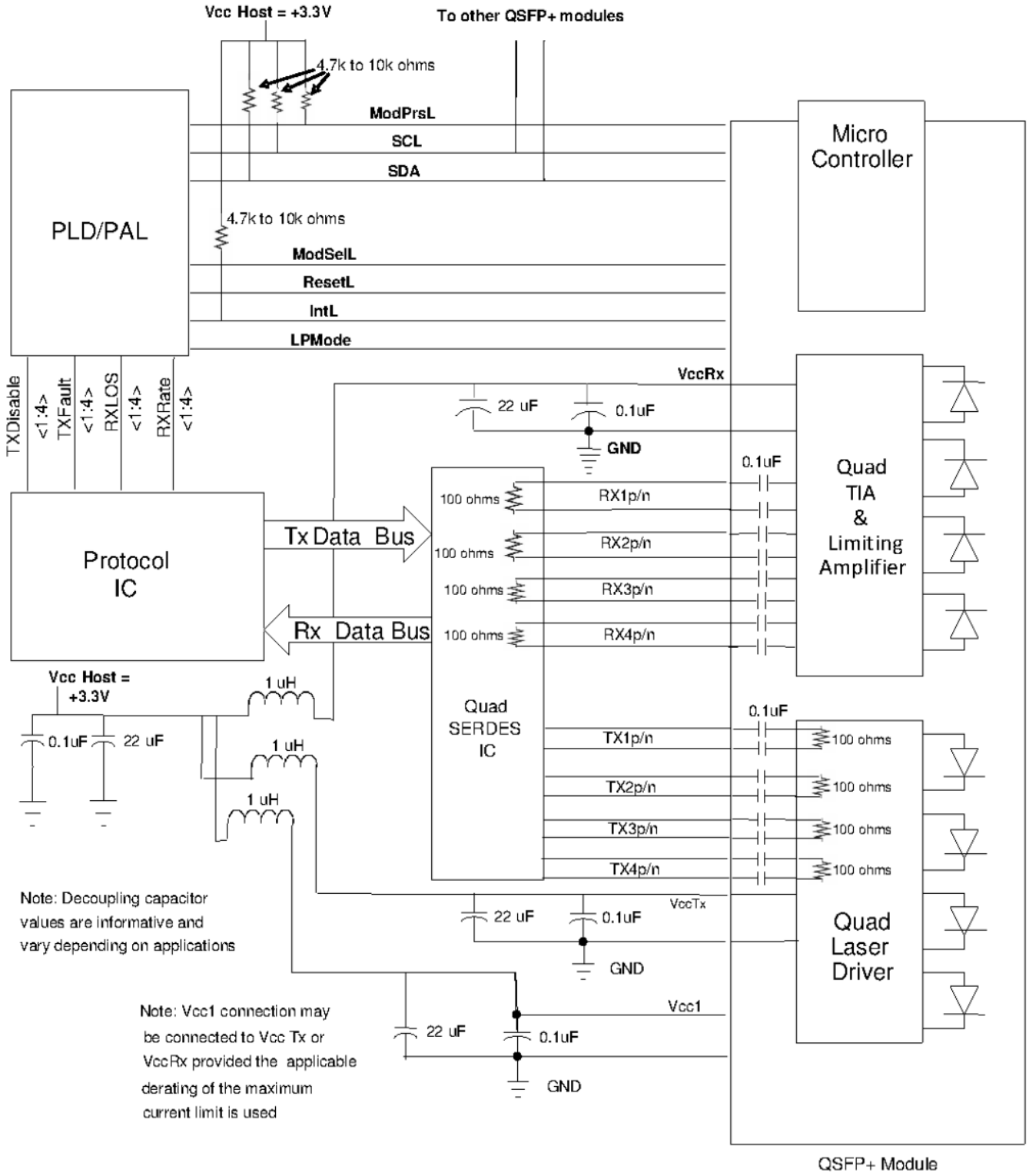


40G QSFP+ PSM LR4 10km Optical Interface



Female MPO Connector with 8-degree End-face for this module

Recommended Circuit



Recommended High-speed Interface Circuit